GD25LQ255E

DATASHEET

Contents

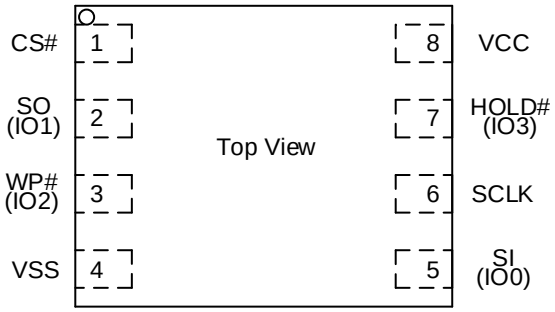
1 FEATURES

- 256M-bit Serial Flash
  - 32M-Byte
  - 256 Bytes per programmable page
- Standard, Dual, Quad SPI, QPI
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#, RESET#
  - Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#, RESET#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3, RESET#
  - QPI: SCLK, CS#, IO0, IO1, IO2, IO3, RESET#
  - 3 or 4-Byte Address Mode
- High Speed Clock Frequency
  - 133MHz for fast read with 30PF load
  - Dual I/O Data transfer up to 266Mbits/s
  - Quad I/O Data transfer up to 532Mbits/s
  - QPI Mode Data transfer up to 532Mbits/s
- Software/Hardware Write Protection
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Top/Bottom Block protection
- Endurance and Data Retention
  - Minimum 100,000 Program/Erase Cycles
  - 20-year data retention typical
- Allows XiP (eXecute In Place) Operation
  - High speed Read reduce overall XiP instruction fetch time
  - Continuous Read with Wrap further reduce data latency to fill up SoC cache
- Fast Program/Erase Speed
  - Page Program time: 0.25ms typical
  - Sector Erase time: 30ms typical
  - Block Erase time: 0.1s/0.15s typical
  - Chip Erase time: 64s typical
- Flexible Architecture
  - Uniform Sector of 4K-Byte
  - Uniform Block of 32/64K-Byte
- Low Power Consumption
  - 11μA typical standby current
  - 1μA typical deep power down current
- Advanced Security Features
  - 128-bit Unique ID for each device
  - Serial Flash Discoverable parameters (SFDP) register
  - 2x1024-Byte Security Registers With OTP Locks
- Single Power Supply Voltage
  - Full voltage range: 1.65-2.0V
- Package Information
  - SOP16 300mil
  - WSON8 (6x5mm)
  - WSON8 (8x6mm)
  - TFBGA-24ball (5x5 Ball Array)
  - WLCSP

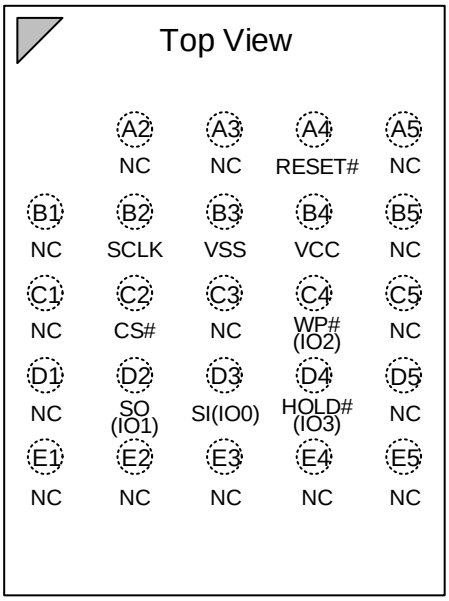
2 GENERAL DESCRIPTIONS

The GD25LQ255E (256M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), I/O3 (HOLD#). The Dual I/O data is transferred with speed of 266Mbit/s, and the Quad I/O data is transferred with speed of 532Mbit/s.

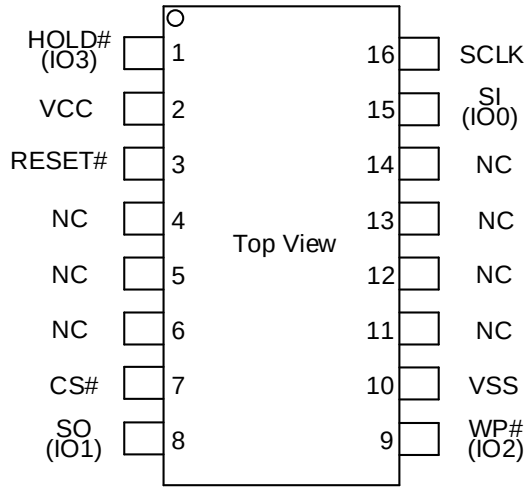
CONNECTION DIAGRAM



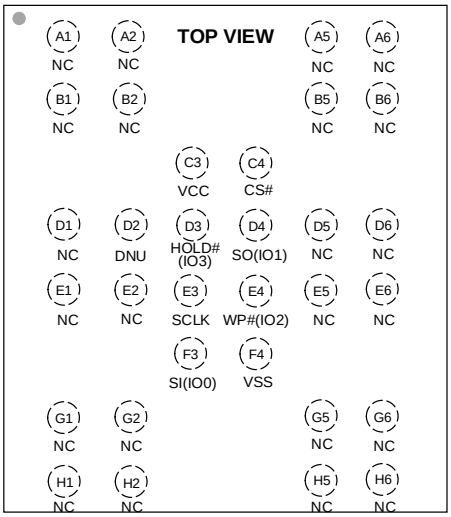
8 - LEAD WSON



24-BALL TFBGA (5x5 ball array)



16-LEAD SOP



WLCSP

PIN DESCRIPTION

Table 1. Pin Description for WSON8 Package

Pin No.	Pin Name	I/O	Description
1	CS#	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1)
3	WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
4	VSS		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0)
6	SCLK	I	Serial Clock Input
7	HOLD# (IO3)	I/O	Hold Input (Data Input Output 3)
8	VCC		Power Supply

Table 2. Pin Description for SOP16 Package

Pin No.	Pin Name	I/O	Description
1	HOLD# (IO3)	I/O	Hold Input (Data Input Output 3)
2	VCC		Power Supply
3	RESET#	I	Reset Input
7	CS#	I	Chip Select Input
8	SO (IO1)	I/O	Data Output (Data Input Output 1)
9	WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
10	VSS		Ground
15	SI (IO0)	I/O	Data Input (Data Input Output 0)
16	SCLK	I	Serial Clock Input

Table 3. Pin Description for TFBGA24 Package

Pin No.	Pin Name	I/O	Description
A4	RESET#	I	Reset Input
B2	SCLK	I	Serial Clock Input
B3	VSS		Ground
B4	VCC		Power Supply
C2	CS#	I	Chip Select Input
C4	WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
D2	SO (IO1)	I/O	Data Output (Data Input Output 1)
D3	SI (IO0)	I/O	Data Input (Data Input Output 0)
D4	HOLD# (IO3)	I/O	Hold Input (Data Input Output 3)

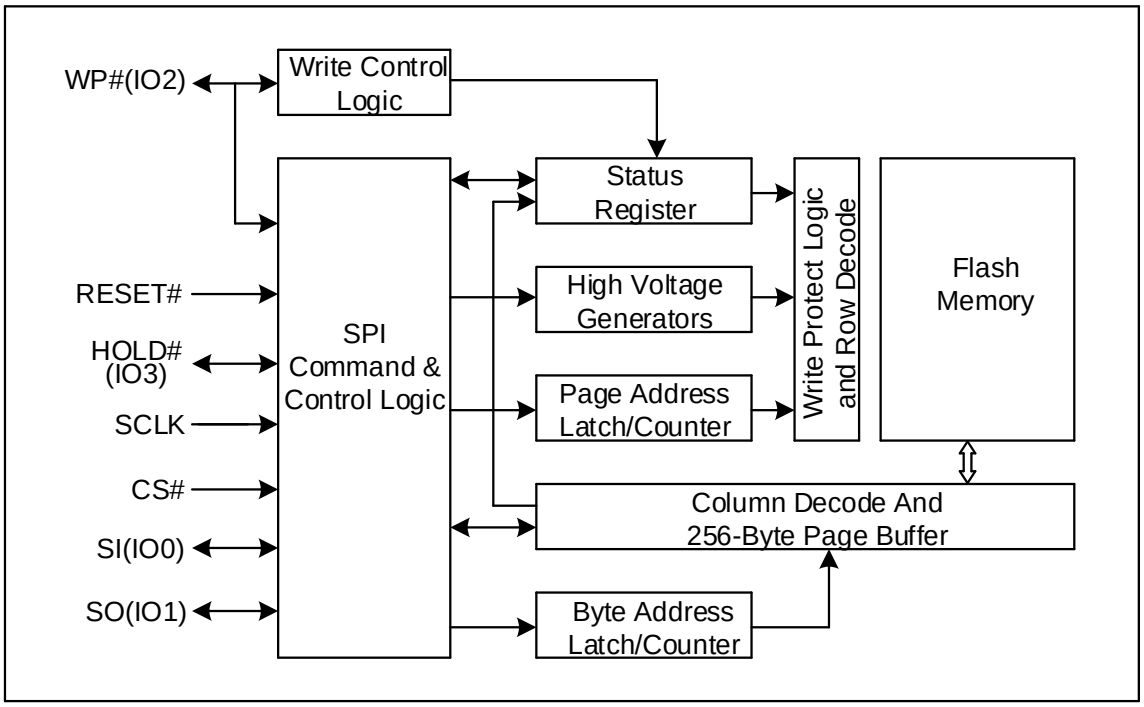
Table 4. Ball Description for WLCSP Package

Pin No.	Pin Name	I/O	Description
C3	VCC		Power Supply
D3	HOLD# (IO3)	I/O	Hold Input (Data Input Output 3)

E3	SCLK	I	Serial Clock Input
F3	SI (IO0)	I/O	Data Input(Data Input Output0)
C4	CS#	I	Chip Select Input
D4	SO (IO1)	I/O	Data Output(Data Input Output1)
E4	WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
F4	VSS		Ground
D2	DNU		Do Not Use
Multiple	NC		No Connection

Note: CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.

BLOCK DIAGRAM



3 MEMORY ORGANIZATION

GD25LQ255E

Each device has	Each block has	Each sector has	Each page has	
32M	64/32K	4K	256	Bytes
128K	256/128	16	-	pages
8K	16/8	-	-	sectors
512/1K	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

GD25LQ255E 64K Bytes Block Sector Architecture

Block	Sector	Address range	
511	8191	1FFF000H	1FFFFFFH
	.....	.....	.....
	8176	1FF0000H	1FF0FFFH
510	8175	1FEF000H	1FEFFFFH
	.....	.....	.....
	8160	1FE0000H	1FE0FFFH
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
2	47	02F000H	02FFFFH
	.....	.....	.....
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	.....	.....	.....
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	.....	.....	.....
	0	000000H	000FFFH

4 DEVICE OPERATIONS

4.1 SPI Mode

Standard SPI

The GD25LQ255E features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The GD25LQ255E supports Dual SPI operation when using the “Dual Output Fast Read”, “Dual Output Fast Read with 4-Byte address”, “Dual I/O Fast Read” and “Dual I/O Fast Read with 4-Byte address” commands (3BH, 3CH, BBH and BCH). These commands allow data to be transferred to or from the device at twice the rate of the standard SPI. When using the Dual SPI command, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The GD25LQ255E supports Quad SPI operation when using the “Quad Output Fast Read”, “Quad Output Fast Read with 4-Byte address”, “Quad I/O Fast Read”, “Quad I/O Fast Read with 4-Byte address” (6BH, 6CH, EBH, ECH) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI commands, the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and the WP# and HOLD# pins become bidirectional I/O pins: IO2 and IO3. The Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register set to 1.

4.2 QPI Mode

The GD25LQ255E supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enable the QPI (38H)” command. The QPI mode utilizes all four IO pins to input the command code. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given times. “Enable the QPI (38H)” and “Disable the QPI (FFH)” commands are used to switch between these two modes. Upon power-up and after software reset using “Reset (99H)” command, the default state of the device is Standard/Dual/Quad SPI mode. The QPI commands require the non-volatile Quad Enable bit (QE) in Status Register set to 1.

4.3 HOLD Function

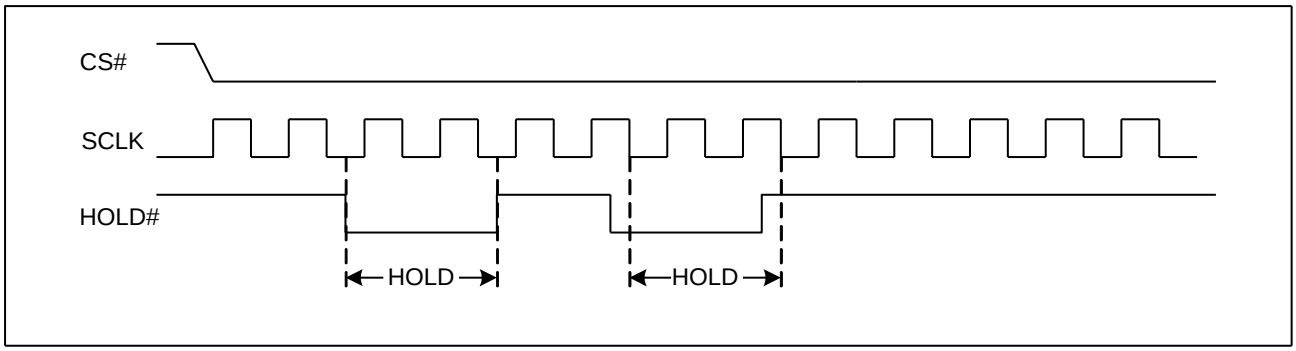
The HOLD function is available when QE=0. If QE=1, The HOLD function is disabled, and the HOLD# pin acts as dedicated data I/O pin.

The HOLD# signal goes low to stop any serial communications with the device, except the operation of write status register, programming, or erasing in progress.

The operation of HOLD needs CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low. If SCLK is not low, HOLD operation will not start until SCLK is low. The HOLD condition ends on rising edge of HOLD# signal with SCLK being low. If SCLK is not low, HOLD operation will not end until SCLK is low.

The SO is high impedance, both SI and SCLK don’t care during the HOLD operation. If CS# is driven high during HOLD operation, it will reset the internal logic of the device. To re-start communication with the chip, the HOLD# must be at high and then CS# must be at low.

Figure 1 HOLD Condition

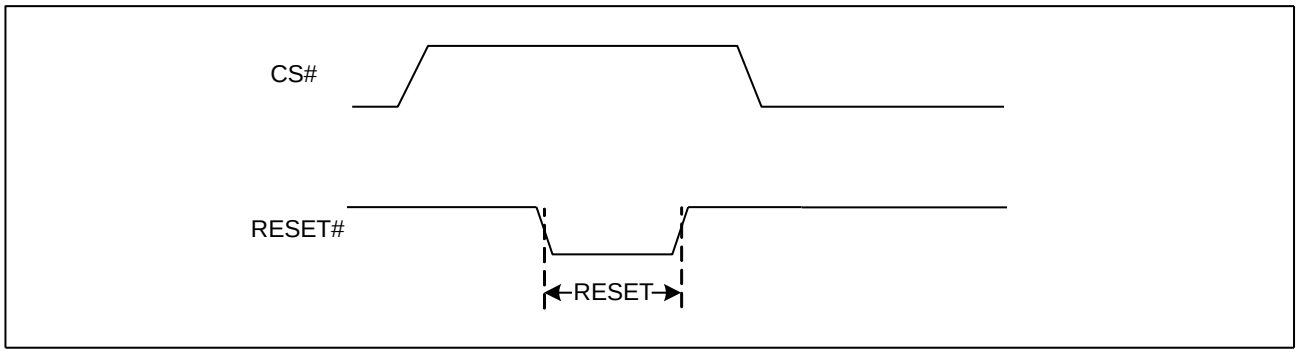


4.4 RESET Function

For 16-pin and 24-ball packages, a dedicated RESET# is used to do the hardware RESET. The RESET# pin goes low for a minimum period of tRLRH (1μs) will reset the flash. After reset cycle, the flash is at the following states:

- Standby mode
- All the volatile bits will return to the default status as power on.

Figure 2 RESET Condition



5 DATA PROTECTION

The GD25LQ255E provide the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  -Power-Up / Software Reset (66H+99H)
  -Write Disable (WRDI)
  -Write Status Register (WRSR)
  -Page Program (PP)
  -Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode: The Block Protect bits (BP4-BP0) define the section of the memory array that can be read but not changed.
- Hardware Protection Mode: WP# goes low to protect the Block Protect bits (BP4-BP0) and the SRP bits (SRP1 and SRP0).
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command and Software Reset (66H+99H).
- Write Inhibit Voltage (VWI): Device would reset automatically when VCC is below a certain threshold VWI.

Table 5. GD25LQ255E Protected area size (CMP=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	504 to 511	1F80000H-1FFFFFFH	512KB	Upper 1/64
0	0	0	1	0	495 to 511	1F00000H-1FFFFFFH	1MB	Upper 1/32
0	0	0	1	1	479 to 511	1E00000H-1FFFFFFH	2MB	Upper 1/16
0	0	1	0	0	447 to 511	1C00000H-1FFFFFFH	4MB	Upper 1/8
0	0	1	0	1	384 to 511	1800000H-1FFFFFFH	8MB	Upper 1/4
0	0	1	1	0	256 to 511	1000000H-1FFFFFFH	16MB	Upper 1/2
0	1	0	0	1	0 to 7	000000H-07FFFFH	512KB	Lower 1/64
0	1	0	1	0	0 to 15	000000H-0FFFFFH	1MB	Lower 1/32
0	1	0	1	1	0 to 31	000000H-1FFFFFH	2MB	Lower 1/16
0	1	1	0	0	0 to 63	000000H-3FFFFFH	4MB	Lower 1/8
0	1	1	0	1	0 to 127	000000H-7FFFFFH	8MB	Lower 1/4
0	1	1	1	0	0 to 255	000000H-0FFFFFFH	16MB	Lower 1/2
X	X	1	1	1	0 to 511	000000H-1FFFFFFH	32MB	ALL
1	0	0	0	1	511	1FFF000H-1FFFFFFH	4KB	Top Block
1	0	0	1	0	511	1FFE000H-1FFFFFFH	8KB	Top Block
1	0	0	1	1	511	1FFC000H-1FFFFFFH	16KB	Top Block
1	0	1	0	X	511	1FF8000H-1FFFFFFH	32KB	Top Block
1	0	1	1	0	511	1FF8000H-1FFFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block

1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block

Table 6. GD25LQ255E Protected area size (CMP=1)

Status Register Content					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
X	X	0	0	0	0 to 511	000000H-1FFFFFFH	ALL	ALL
0	0	0	0	1	0 to 503	000000H-1F7FFFFH	32256KB	Lower 63/64
0	0	0	1	0	0 to 494	000000H-1EFFFFFH	31MB	Lower 31/32
0	0	0	1	1	0 to 478	000000H-1DFFFFFH	30MB	Lower 15/16
0	0	1	0	0	0 to 446	000000H-1BFFFFFH	28MB	Lower 7/8
0	0	1	0	1	0 to 383	000000H-17FFFFFH	24MB	Lower 3/4
0	0	1	1	0	0 to 254	000000H-0FFFFFFH	16MB	Lower 1/2
0	1	0	0	1	8 to 511	080000H-1FFFFFFH	32256KB	Upper 63/64
0	1	0	1	0	16 to 511	100000H-1FFFFFFH	31MB	Upper 31/32
0	1	0	1	1	32 to 511	200000H-1FFFFFFH	30MB	Upper 15/16
0	1	1	0	0	64 to 511	400000H-1FFFFFFH	28MB	Upper 7/8
0	1	1	0	1	128 to 511	800000H-1FFFFFFH	24MB	Upper 3/4
0	1	1	1	0	256 to 511	1000000H-1FFFFFFH	16MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 511	000000H-1FFEFFFH	32764KB	L-4095/4096
1	0	0	1	0	0 to 511	000000H-1FFDFFFH	32760KB	L-2047/2048
1	0	0	1	1	0 to 511	000000H-1FFBFFFH	32752KB	L-1023/1024
1	0	1	0	X	0 to 511	000000H-1FF7FFFH	32736KB	L-511/512
1	0	1	1	0	0 to 511	000000H-1FF7FFFH	32736KB	L-511/512
1	1	0	0	1	0 to 511	001000H-1FFFFFFH	32764KB	U-4095/4096
1	1	0	1	0	0 to 511	002000H-1FFFFFFH	32760KB	U-2047/2048
1	1	0	1	1	0 to 511	004000H-1FFFFFFH	32752KB	U-1023/1024
1	1	1	0	X	0 to 511	008000H-1FFFFFFH	32736KB	U-511/512
1	1	1	1	0	0 to 511	008000H-1FFFFFFH	32736KB	U-511/512

6 REGISTERS

6.1 Status Register

Table 7. Status Register-SR No.1

No.	Name	Description	Note
S7	SRP0	Status Register Protection Bit	Non-volatile writable
S6	BP4	Block Protect Bit	Non-volatile writable
S5	BP3	Block Protect Bit	Non-volatile writable
S4	BP2	Block Protect Bit	Non-volatile writable
S3	BP1	Block Protect Bit	Non-volatile writable
S2	BP0	Block Protect Bit	Non-volatile writable
S1	WEL	Write Enable Latch	Volatile, read only
S0	WIP	Erase/Write In Progress	Volatile, read only

Table 8. Status Register-SR No.2

No.	Name	Description	Note
S15	SUS1	Erase Suspend Bit	Volatile, read only
S14	CMP	Complement Protect Bit	Non-volatile writable
S13	LB3	Security Register Lock Bit	Non-volatile writable (OTP)
S12	LB2	Security Register Lock Bit	Non-volatile writable (OTP)
S11	ADS	Current Address Mode Bit	Volatile, read only
S10	SUS2	Program Suspend Bit	Volatile, read only
S9	QE	Quad Enable Bit	Non-volatile writable
S8	SRP1	Status Register Protection Bit	Non-volatile writable

The status and control bits of the Status Register are as follows:

WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits

The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table 5&6)

becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1, and BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1, and BP0) bits are 1 and CMP=1.

SRP1, SRP0 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

SRP1	SRP0	#WP	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
0	1	0	Hardware Protected	WP#=0, the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down(1)(2)	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be written to.

NOTE:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact GigaDevice for details.

QE bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (It is best to set the QE bit to 0 to avoid short issues if the WP# or HOLD# pin is tied directly to the power supply or ground.)

ADS bit

The Address Status (ADS) bit is a read only bit that indicates the current address mode the device is operating in. The device is in 3-Byte address mode when ADS=0 (default), and in 4-Byte address mode when ADS=1.

LB3, LB2 bits

The LB3 and LB2 bits are non-volatile One Time Program (OTP) bits in Status Register (S13 and S12) that provide the write protect control and status to the Security Registers. The default state of LB3 and LB2 bits are 0, the security registers are unlocked. The LB3 and LB2 bits can be set to 1 individually using the Write Register instruction. The LB3 and LB2 bits are One Time Programmable, once they are set to 1, the Security Registers will become read-only permanently.

CMP bit

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction with the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The

default setting is CMP=0.

SUS1, SUS2 bits

The SUS1 and SUS2 bits are read only bits in the status register (S15 and S10) that are set to 1 after executing an Erase/ Program Suspend (75H) command (The Erase Suspend will set the SUS1 bit to 1, and the Program Suspend will set the SUS2 bit to 1). The SUS1 and SUS2 bits are cleared to 0 by Erase/Program Resume (7AH) command, software reset (66H+99H) command, as well as a power-down, power-up cycle.

6.2 Extended Address Register

Table 9. Extended Address Register

No.	Name	Description	Note
EA7	Reserved	Reserved	Reserved
EA6	Reserved	Reserved	Reserved
EA5	Reserved	Reserved	Reserved
EA4	Reserved	Reserved	Reserved
EA3	Reserved	Reserved	Reserved
EA2	Reserved	Reserved	Reserved
EA1	Reserved	Reserved	Reserved
EA0	A24	Address bit	Volatile writable

The bits of the Extended Address Register are as follows:

A24 bit

The Extended Address Bits are used only when the device is operating in the 3-Byte Address Mode, which are volatile writable by C5H command.

A24	Address
0	0000 0000h-00FF FFFFh
1	0100 0000h-01FF FFFFh

If an “Enter 4-Byte Address Mode (B7H)” instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Bit setting will be ignored.

Reserved bit

It is recommended to set the value of the reserved bit as “0”.

7 COMMAND DESCRIPTIONS

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, with most significant bit first on SI, and each bit is latched on the rising edges of SCLK.

Every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read instruction can be completed after any bit of the data-out sequence is being shifted out, and then CS# must be driven high to return to deselected status.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 10. Commands (SPI, 3- or 4-Byte Addr. Mode)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Write Enable	06H								
Write Disable	04H								
Read Status Register-1	05H	(S7-S0)	(cont.)						
Read Status Register-2	35H	(S15-S8)	(cont.)						
Write Status Register-1&2	01H	S7-S0	S15-S8						
Read Extended Addr. Register	C8H	(EA7-EA0)							
Write Extended Addr. Register	C5H	EA7-EA0							
Volatile SR write Enable	50H								
Fast Read with 4-Byte Address	0CH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)	
Set Burst with Wrap	77H	dummy(1)	dummy(1)	dummy(1)	W7-W0(1)				
Chip Erase	C7/60H								
Enter 4-Byte Address Mode	B7H								
Exit 4-Byte Address Mode	E9H								
Read Manufacturer/ Device ID	90H	00H	00H	00H	(MID7-MID0)	(ID7-ID0)	(cont.)		

Read Identification	9FH	(MID7-MID0)	(ID15-ID8)	(ID7-ID0)	(cont.)				
Enable Reset	66H								
Reset	99H								
Program/Erase Suspend	75H								
Program/Erase Resume	7AH								
Deep Power-Down	B9H								
Release From Deep Power-Down	ABH								
Release From Deep Power-Down and Read Device ID	ABH	dummy	dummy	dummy	(ID7-ID0)	(cont.)			
Enable QPI	38H								
Read Serial Flash Discoverable Parameter	5AH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Read Data with 4-Byte Address	13H	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)		
Fast Read Dual Output with 4-Byte Address	3CH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(2)	(cont.)	
Fast Read Quad Output with 4-Byte Address	6CH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)	(cont.)	
Fast Read Dual I/O with 4-Byte Address	BCH	A31-A24(4)	A23-A16(4)	A15-A8(4)	A7-A0(4)	M7-M0(5)	(D7-D0)(2)	(cont.)	
Fast Read Quad I/O with 4-Byte Address	ECH	A31-A24(6)	A23-A16(6)	A15-A8(6)	A7-A0(6)	M7-M0(7)	dummy	dummy	(D7-D0)(3)
Page Program with 4-Byte Address	12H	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte		
Quad Page Program with 4-Byte Address	34H	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0(8)	Next Byte		
Sector Erase with 4-Byte Address	21H	A31-A24	A23-A16	A15-A8	A7-A0				
Block Erase (32K) with 4-Byte Address	5CH	A31-A24	A23-A16	A15-A8	A7-A0				
Block Erase (64K) with 4-Byte Address	DCH	A31-A24	A23-A16	A15-A8	A7-A0				

Table 11. Commands (SPI, 3-Byte Addr. Mode)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)			
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(2)	(cont.)		
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)	(cont.)		
Dual I/O Fast Read	BBH	A23-A16(9)	A15-A8(9)	A7-A0(9)	M7-M0(5)	(D7-D0)(2)	(cont.)		
Quad I/O Fast Read	EBH	A23-A16(10)	A15-A8(10)	A7-A0(10)	M7-M0(7)	dummy	dummy	(D7-D0)(3)	(cont.)
Page Program	02H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Quad Page Program	32H	A23-A16	A15-A8	A7-A0	D7-D0(8)	Next Byte			
Sector Erase	20H	A23-A16	A15-A8	A7-A0					
Block Erase (32K)	52H	A23-A16	A15-A8	A7-A0					
Block Erase (64K)	D8H	A23-A16	A15-A8	A7-A0					
Read Unique ID	4BH	00H	00H	00H	dummy	(UID7-UID0)	(cont.)		
Erase Security Registers(11)	44H	A23-A16	A15-A8	A7-A0					
Program Security Registers(11)	42H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte			
Read Security Registers(11)	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)		

Table 12. Commands (SPI, 4-Byte Addr. Mode)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Read Data	03H	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(cont.)		
Fast Read	0BH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)	
Dual Output Fast Read	3BH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(2)	(cont.)	
Quad Output Fast Read	6BH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)	(cont.)	
Dual I/O Fast Read	BBH	A31-A24(4)	A23-A16(4)	A15-A8(4)	A7-A0(4)	M7-M0(5)	(D7-D0)(2)	(cont.)	
Quad I/O Fast Read	EBH	A31-A24(6)	A23-A16(6)	A15-A8(6)	A7-A0(6)	M7-M0(6)	dummy	dummy	(D7-D0)(3)
Page Program	02H	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte		
Quad Page Program	32H	A31-A24(6)	A23-A16(6)	A15-A8(6)	A7-A0(6)	D7-D0(8)	Next Byte		
Sector Erase	20H	A31-A24	A23-A16	A15-A8	A7-A0				
Block Erase (32K)	52H	A31-A24	A23-A16	A15-A8	A7-A0				
Block Erase (64K)	D8H	A31-A24	A23-A16	A15-A8	A7-A0				

Read Unique ID	4BH	00H	00H	00H	00H	dummy	(UID7-UID0)	(cont.)	
Erase Security Registers(11)	44H	A31-A24	A23-A16	A15-A8	A7-A0				
Program Security Registers(11)	42H	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte		
Read Security Registers(11)	48H	A31-A24	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(cont.)	

Table 13. Commands (QPI, 3- or 4-Byte Addr. Mode)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number	(0,1)	(2,3)	(4,5)	(6,7)	(8,9)	(10,11)	(12,13)	(14,15)
Write Enable	06H							
Write Disable	04H							
Read Status Register-1	05H	(S7-S0)						
Read Status Register-2	35H	(S15-S8)						
Write Status Register-1&2	01H	S7-S0	S15-S8					
Read Extended Addr. Register	C8H	(EA7-EA0)						
Write Extended Addr. Register	C5H	EA7-EA0						
Volatile SR Write Enable	50H							
Set Read Parameters	C0H	P7-P0						
Chip Erase	C7/60H							
Enter 4-Byte Address Mode	B7H							
Exit 4-Byte Address Mode	E9H							
Manufacturer/Device ID	90H	dummy	dummy	00H	(MID7-MID0)	(ID7-ID0)	(cont.)	
Read Identification	9FH	(MID7-MID0)	(ID15-ID8)	(ID7-ID0)	(cont.)			
Enable Reset	66H							
Reset	99H							
Program/Erase Suspend	75H							
Program/Erase Resume	7AH							
Deep Power-Down	B9H							
Release From Deep Power-Down	ABH							
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(ID7-ID0)	(cont.)		
Disable QPI	FFH							

Read Serial Flash Discoverable Parameter	5AH	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)	(cont.)
Fast Read Quad I/O with 4-Byte Address	ECH	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	dummy	(D7-D0)
Page Program with 4-Byte Address	12H	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte	
Sector Erase with 4-Byte Address	21H	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase (32K) with 4-Byte Address	5CH	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase (64K) with 4-Byte Address	DCH	A31-A24	A23-A16	A15-A8	A7-A0			

Table 14. Commands (QPI, 3-Byte Addr. Mode)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number	(0,1)	(2,3)	(4,5)	(6,7)	(8,9)	(10,11)	(12,13)	(14,15)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)	(cont.)
Quad I/O Fast Read	EBH	A23-A16	A15-A8	A7-A0	M7-M0	dummy	(D7-D0)	(cont.)
Burst Read with Wrap	0CH	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)	(cont.)
Page Program	02H	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte		
Sector Erase	20H	A23-A16	A15-A8	A7-A0				
Block Erase (32K)	52H	A23-A16	A15-A8	A7-A0				
Block Erase (64K)	D8H	A23-A16	A15-A8	A7-A0				

Table 15. Commands (QPI, 4-Byte Addr. Mode)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number	(0,1)	(2,3)	(4,5)	(6,7)	(8,9)	(10,11)	(12,13)	(14,15)
Fast Read	0BH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)
Quad I/O Fast Read	EBH	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	dummy	(D7-D0)
Burst Read with Wrap	0CH	A31-A24	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)
Page Program	02H	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	Next Byte	
Sector Erase	20H	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase (32K)	52H	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase (64K)	D8H	A31-A24	A23-A16	A15-A8	A7-A0			

Note:

1. Dummy bits and Wrap Bits

IO0 = (x, x, x, x, x, x, W4, x)

IO1 = (x, x, x, x, x, x, W5, x)

IO2 = (x, x, x, x, x, x, W6, x)

IO3 = (x, x, x, x, x, x, x, x)

2. Dual Output data

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

3. Quad Output Data

IO0 = (D4, D0, …)

IO1 = (D5, D1, …)

IO2 = (D6, D2, …)

IO3 = (D7, D3, …)

4. Dual Input 4-Byte Address

IO0 = A30, A28, A26, A24, A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0

IO1 = A31, A29, A27, A25, A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1

5. Dual Input Mode bit

IO0 = M6, M4, M2, M0

IO1 = M7, M5, M3, M1

6. Quad Input 4-Byte Address

IO0 = A28, A24, A20, A16, A12, A8, A4, A0

IO1 = A29, A25, A21, A17, A13, A9, A5, A1

IO2 = A30, A26, A22, A18, A14, A10, A6, A2

IO3 = A31, A27, A23, A19, A15, A11, A7, A3

7. Quad Input Mode bit

IO0 = M4, M0

IO1 = M5, M1

IO2 = M6, M2

IO3 = M7, M3

8. Quad Output Data

IO0 = D4, D0, …

IO1 = D5, D1, …

IO2 = D6, D2, …

IO3 = D7, D3, …

9. Dual Input Address

IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1

10. Quad Input Address

IO0 = A20, A16, A12, A8, A4, A0

IO1 = A21, A17, A13, A9, A5, A1

IO2 = A22, A18, A14, A10, A6, A2

IO3 = A23, A19, A15, A11, A7, A3

11. Security Registers Address

Security Register2: A23-A16=00H, A15-A12=2H, A11-A10 = 00b, A9-A0= Byte Address;

Security Register3: A23-A16=00H, A15-A12=3H, A11-A10 = 00b, A9-A0= Byte Address;

12. QPI Command, Address, Data input/output format:

CLK #0	1	2	3	4	5	6	7	8	9	10	11
IO0=	C4,	C0,	A20,	A16,	A12,	A8,	A4,	A0,	D4,	D0,	D4, D0,
IO1=	C5,	C1,	A21,	A17,	A13,	A9,	A5,	A1,	D5,	D1,	D5, D1

IO2= C6, C2, A22, A18, A14, A10, A6, A2, D6, D2, D6, D2
IO3= C7, C3, A23, A19, A15, A11, A7, A3, D7, D3, D7, D3

TABLE OF ID DEFINITIONS

GD25LQ255E

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	C8	60	19
90H	C8		18
ABH			18

7.1 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR) and Erase/Program Security Registers command.

The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

Figure 3. Write Enable Sequence Diagram (SPI)

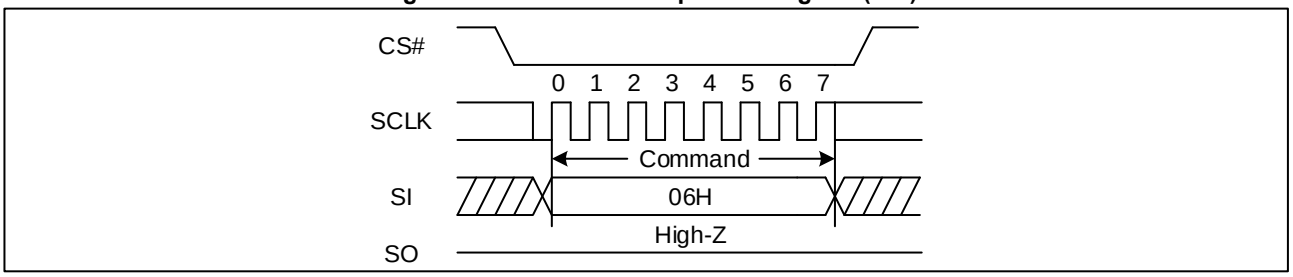
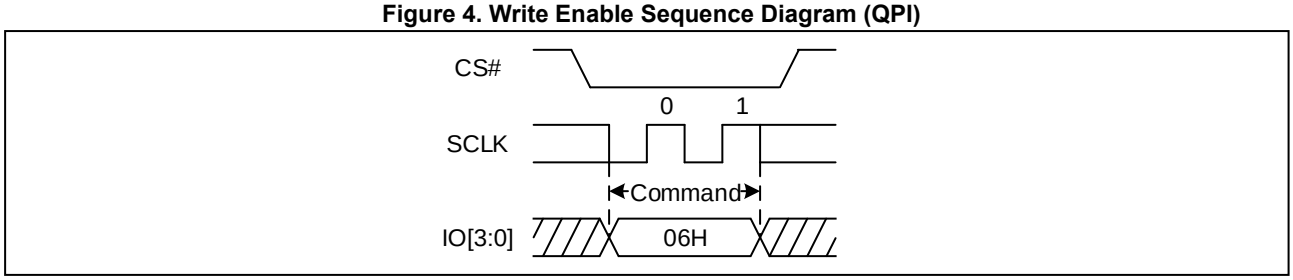


Figure 4. Write Enable Sequence Diagram (QPI)



7.2 Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit may be set to 0 by issuing the Write Disable (WRDI) command to disable Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), that require WEL be set to 1 for execution. The WRDI command can be used by the user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory. The WRDI command is ignored during an embedded operation while WIP bit =1.

The WEL bit is reset by following condition: Write Disable command (WRDI), Power-up, and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

The Write Disable command sequence: CS# goes low →Sending the Write Disable command →CS# goes high.

Figure 5. Write Disable Sequence Diagram (SPI)

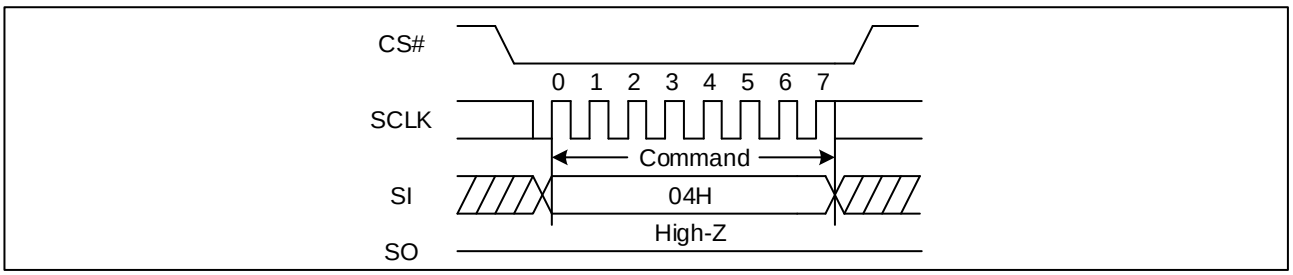
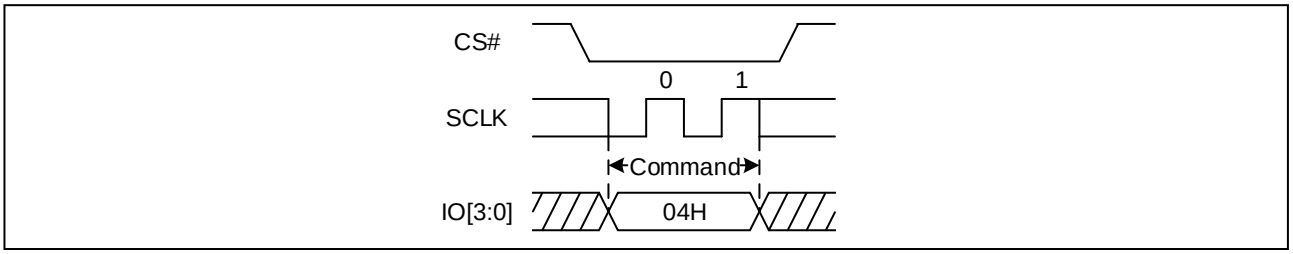


Figure 6. Write Disable Sequence Diagram (QPI)



7.3 Read Status Register (RDSR) (05H or 35H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H” / “35H”, the SO will output Status Register bits S7~S0 / S15~S8.

Figure 7. Read Status Register Sequence Diagram (SPI)

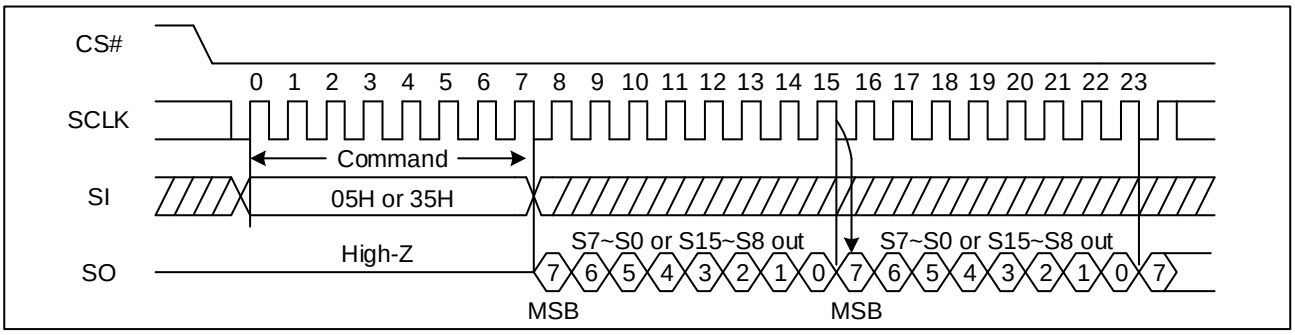
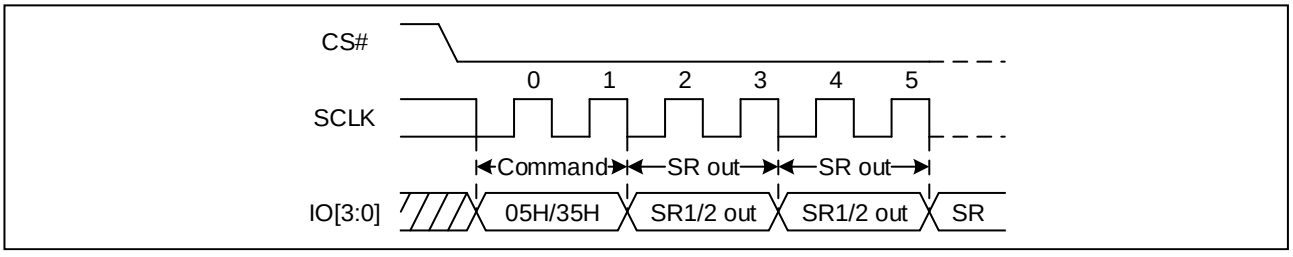


Figure 8. Read Status Register Sequence Diagram (QPI)



7.4 Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S15, S11, S10, S1 and S0 of the Status Register. CS# must be driven high after the eighth or sixteen bit of the data byte has been latched in. Otherwise, the Write Status Register (WRSR) command is not executed. If CS# is driven high after eighth bit of the data byte, the alterable bits in Status Register-2 (S15~S8) will be cleared to 0. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

Figure 9. Write Status Register Sequence Diagram (SPI)

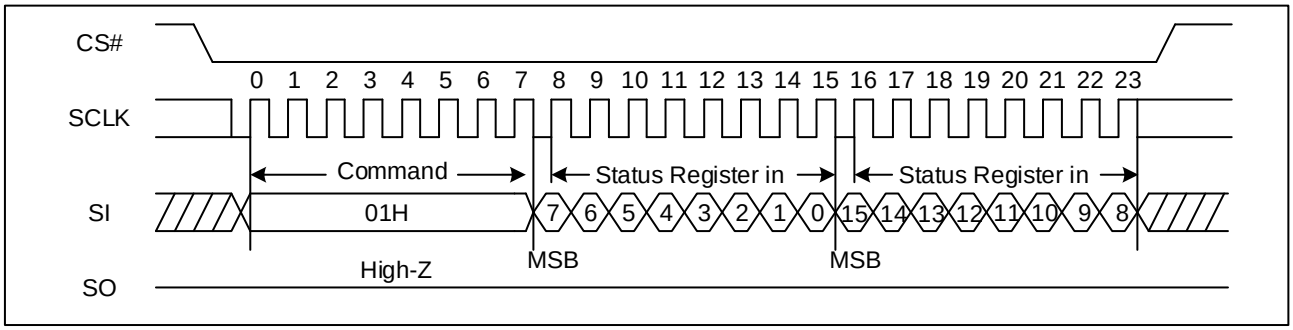
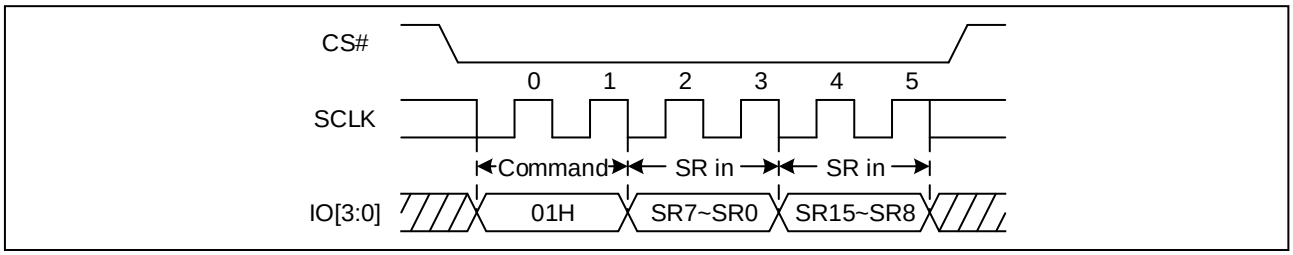


Figure 10. Write Status Register Sequence Diagram (QPI)



7.5 Read Extended Address Register (C8H)

The Read Extended Address Register instruction is entered by driving CS# low and shifting the instruction code “C8H” into the SI pin on the rising edge of SCLK. The Extended Register bits are then shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first.

Figure 11 Read Extended Register Sequence Diagram (SPI)

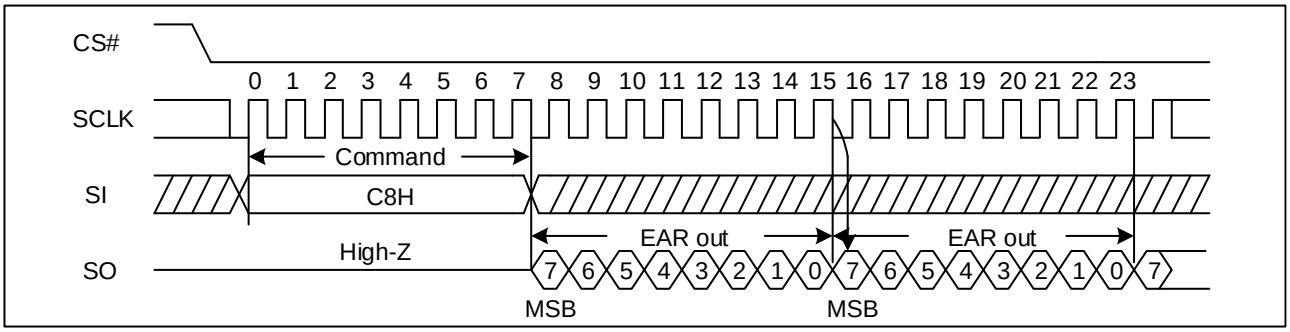
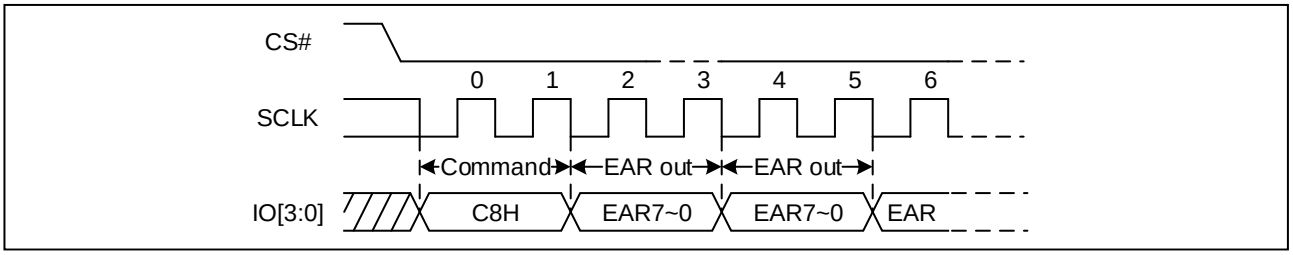


Figure 12 Read Extended Register Sequence Diagram (QPI)



7.6 Write Extended Address Register (C5H)

The Write Extended Address Register command allows new Address bit values to be written to the Extended Address Register. A Write Enable (WREN) instruction must be executed previously to set the Write Enable Latch (WEL) bit before it can be accepted.

The Write Extended Address Register instruction is entered by driving CS# low, sending the instruction code “C5H”, and then writing the Extended Register data Byte.

Upon power up or the execution of a Software/Hardware Reset, the Extended Address Register bit values will be cleared to 0.

Figure 13 Write Extended Address Register Sequence Diagram (SPI)

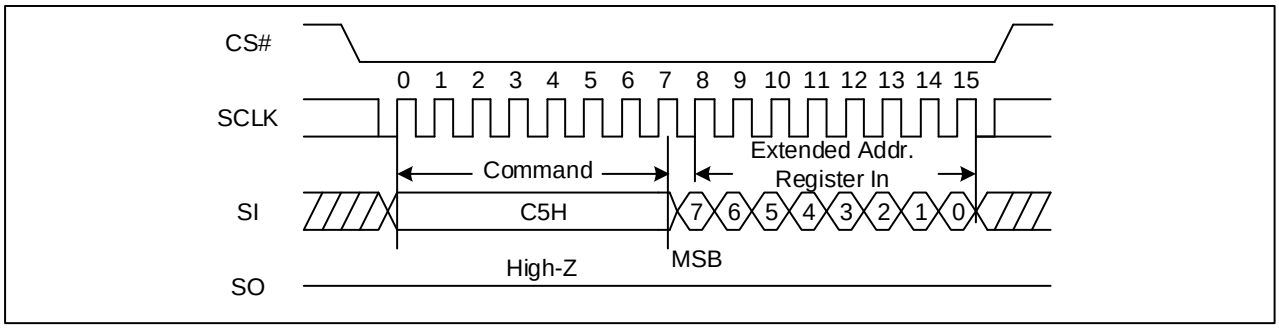
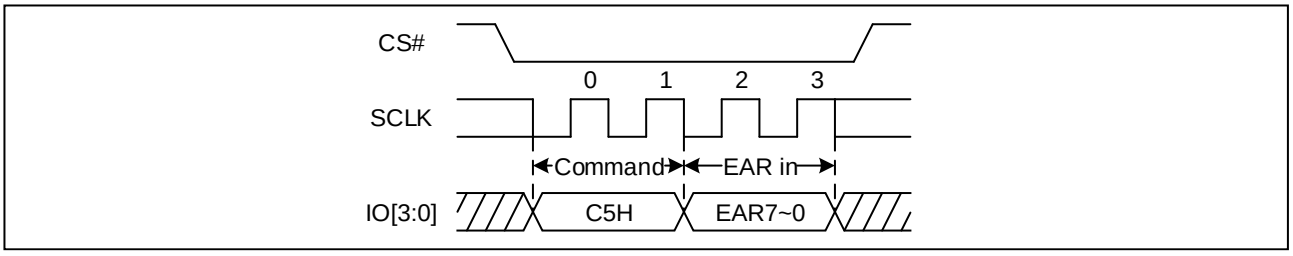


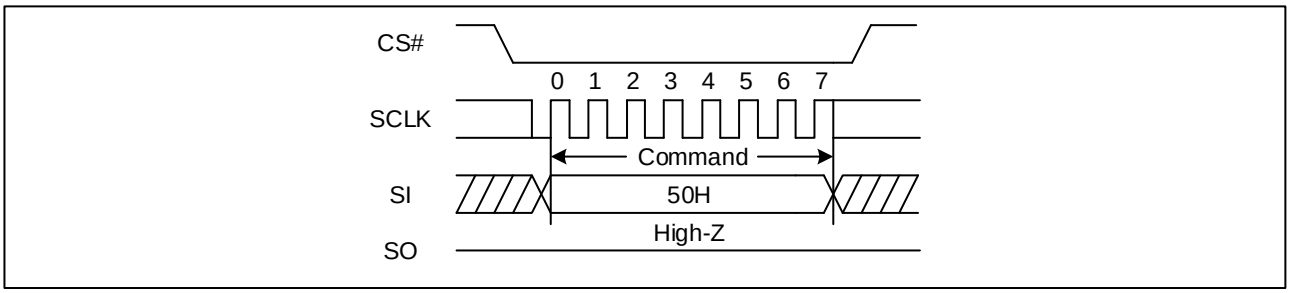
Figure 14 Write Extended Address Register Sequence Diagram (QPI)



7.7 Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can’t be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

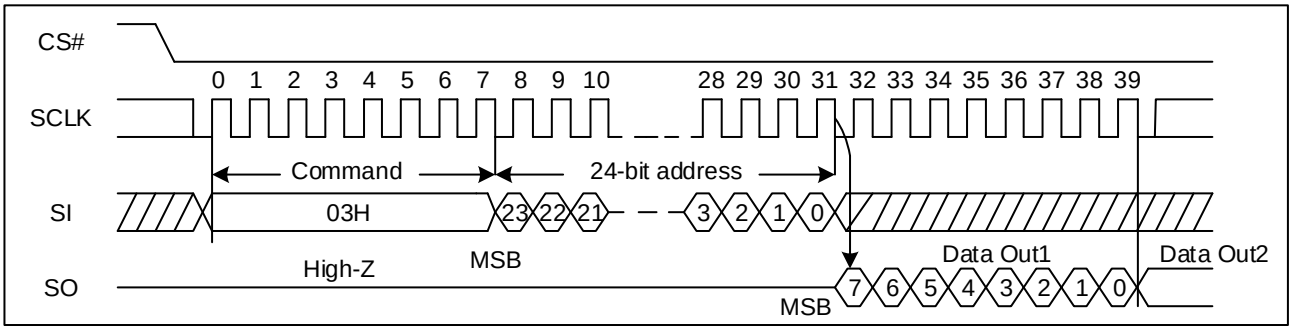
Figure 15. Write Enable for Volatile Status Register Sequence Diagram



7.8 Read Data Bytes (READ) (03H/13H)

The Read Data Bytes (READ) command is followed by a 3- or 4-Byte address (A23-A0 or A31-A0), and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_R, on the falling edge of SCLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 16. Read Data Bytes Sequence Diagram



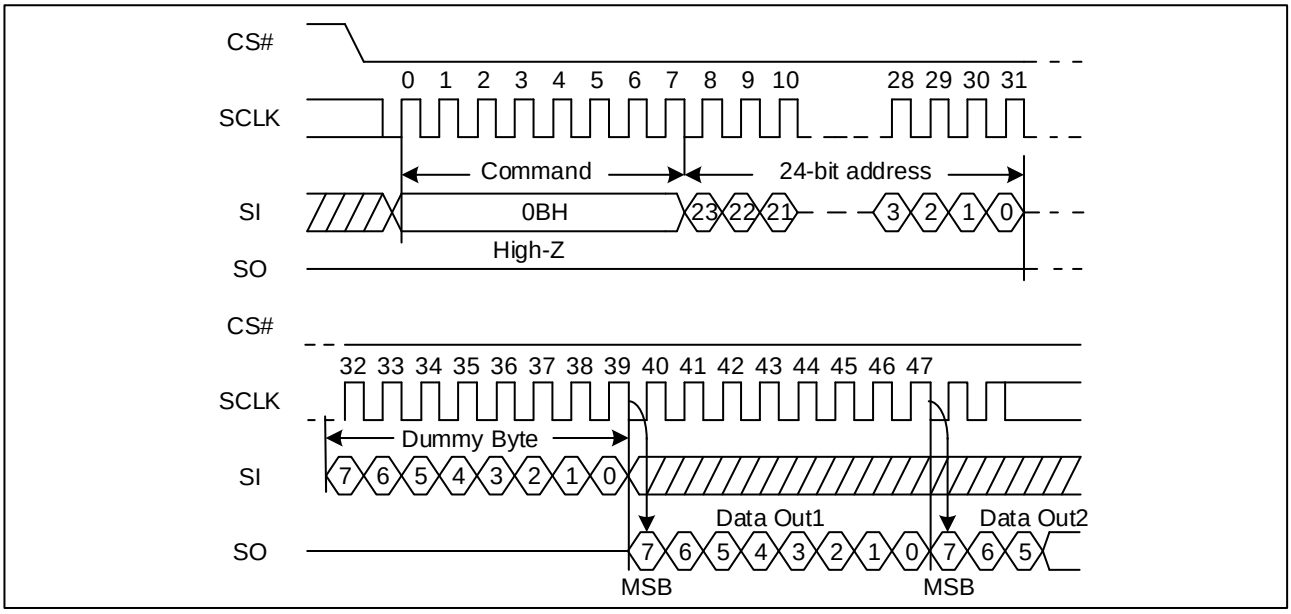
Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

7.9 Read Data Bytes at Higher Speed (Fast Read) (0BH/0CH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3- or 4-Byte address (A23-A0 or A31-A0) and a dummy Byte, and each bit is latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_C, on the falling edge of SCLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

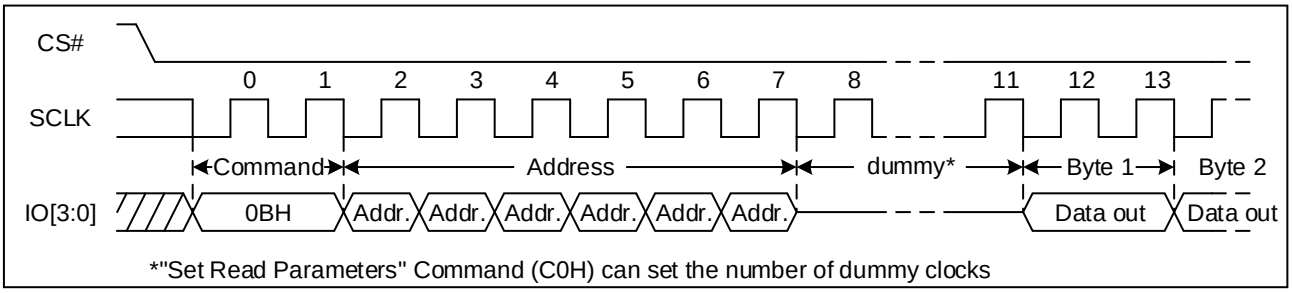
The Fast Read command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the “Set Read Parameters (C0H)” command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P5,P4 setting, the number of dummy clocks can be configured.

Figure 17. Read Data Bytes at Higher Speed Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

Figure 18. Read Data Bytes at Higher Speed Sequence Diagram (QPI)



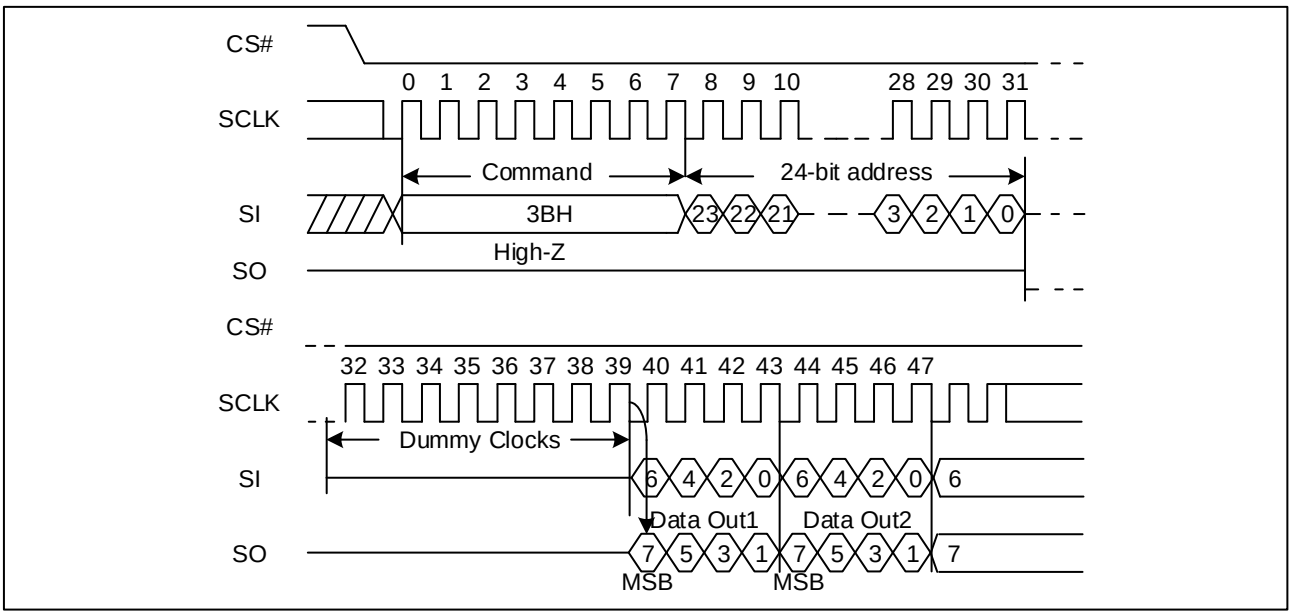
Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

7.10 Dual Output Fast Read (3BH/3CH)

The Dual Output Fast Read command is followed by 3- or 4-Byte address (A23-A0 or A31-A0) and a dummy Byte, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO.

The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Figure 19. Dual Output Fast Read Sequence Diagram

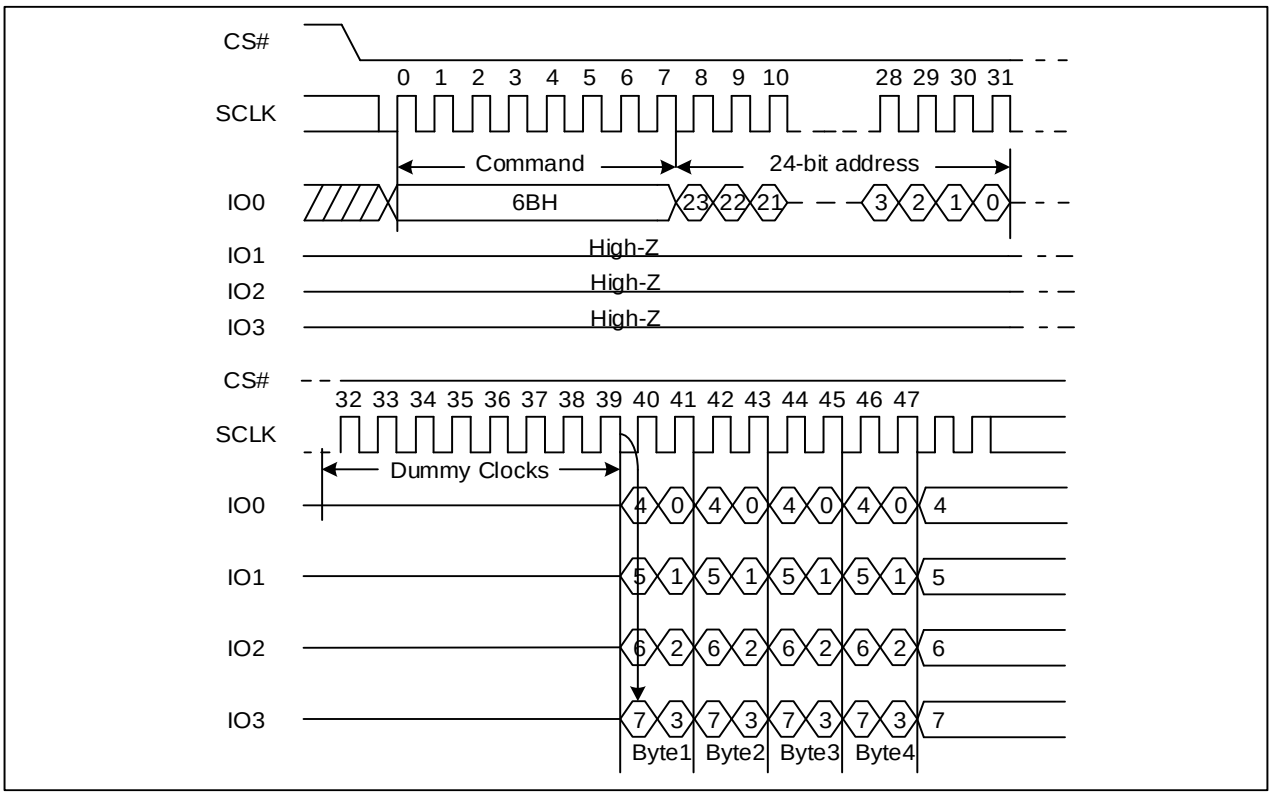


Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

7.11 Quad Output Fast Read (6BH/6CH)

The Quad Output Fast Read command is followed by 3- or 4-Byte address (A23-A0 or A31-A0) and a dummy byte, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad Output Fast Read command.

Figure 20. Quad Output Fast Read Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

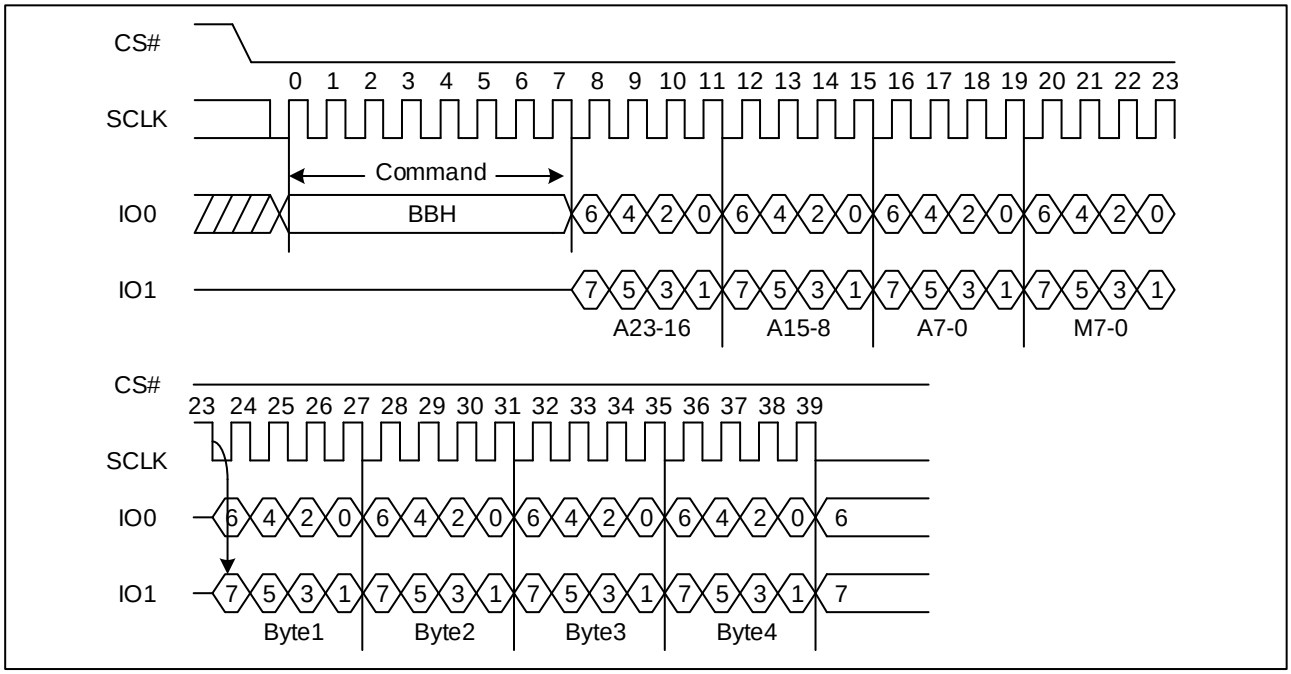
7.12 Dual I/O Fast Read (BBH/BCH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3- or 4-Byte address (A23-A0 or A31-A0) and a "Continuous Read Mode" byte 2-bit per clock by SI and SO, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read with "Continuous Read Mode"

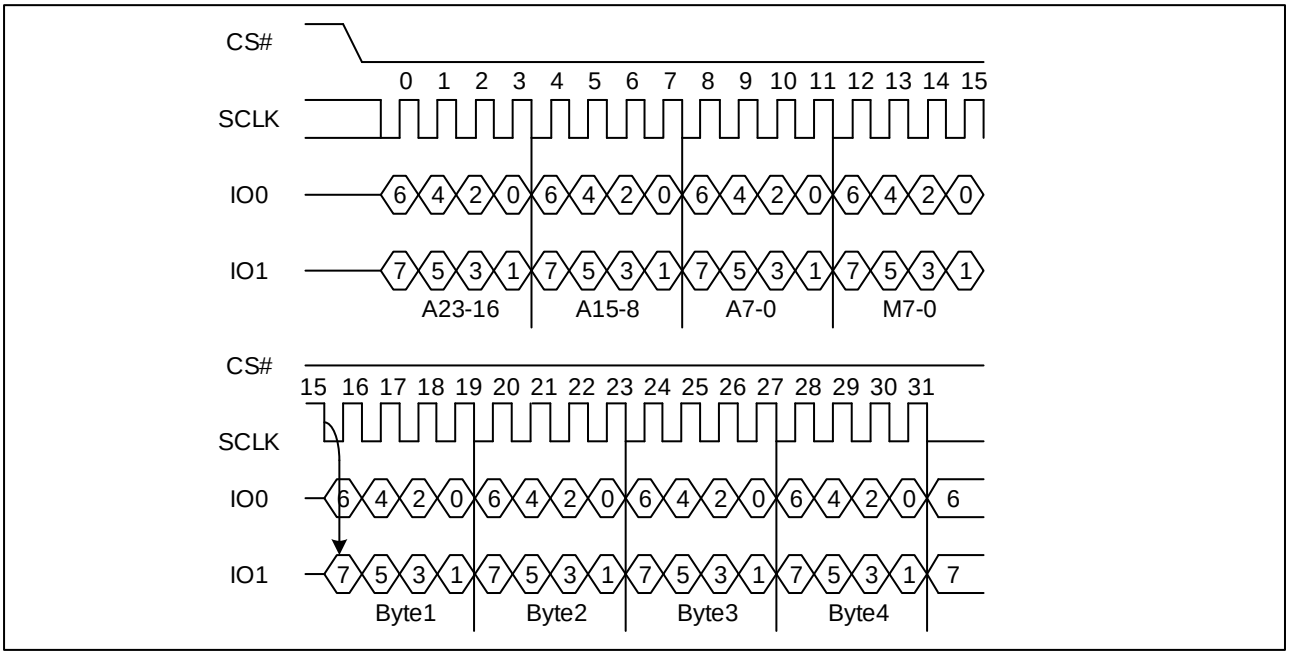
The Dual I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3- or 4-Byte address (A23-A0 or A31-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. If the "Continuous Read Mode" bits (M5-4) do not equal (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be also used to reset (M7-0) before issuing normal command.

Figure 21. Dual I/O Fast Read Sequence Diagram ((M5-4) ≠ (1, 0))



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

Figure 22. Dual I/O Fast Read Sequence Diagram ((M5-4) = (1, 0))



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

7.13 Quad I/O Fast Read (EBH/ECH)

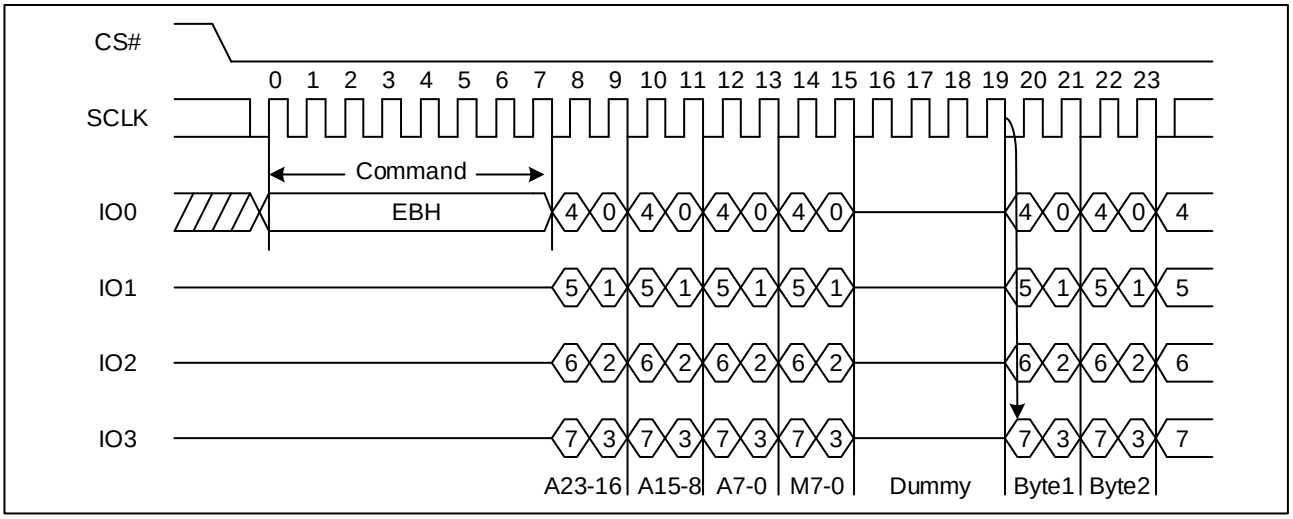
The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3- or 4-Byte address (A23-A0 or A31-A0) and a "Continuous Read Mode" byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

The Quad I/O Fast Read command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P5~P4 setting, the number of dummy clocks can be configured. In QPI mode, the "Continuous Read Mode" bits M7-M0 are also considered as dummy clocks. "Continuous Read Mode" feature is also available in QPI mode for Quad I/O Fast Read command. "Wrap Around" feature is not available in QPI mode for Quad I/O Fast Read command. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0CH) command must be used.

Quad I/O Fast Read with "Continuous Read Mode"

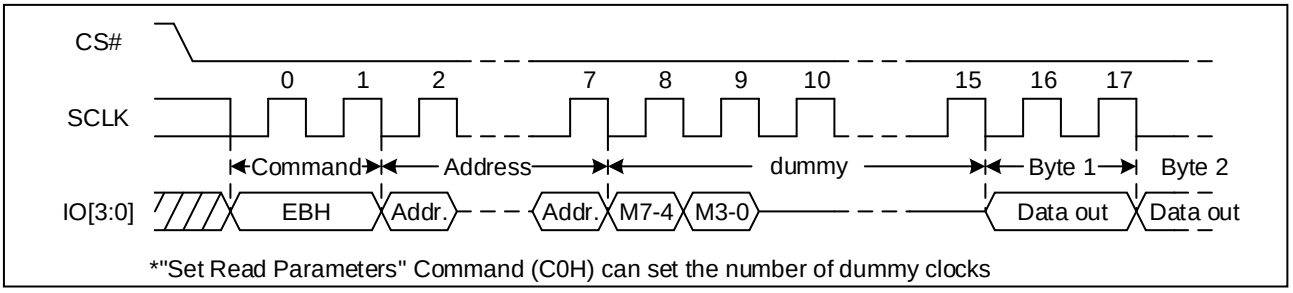
The Quad I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3- or 4-Byte address (A23-A0 or A31-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. If the "Continuous Read Mode" bits (M5-4) do not equal to (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be also used to reset (M7-0) before issuing normal command.

Figure 23. Quad I/O Fast Read Sequence Diagram ((M5-4) ≠ (1, 0), SPI)



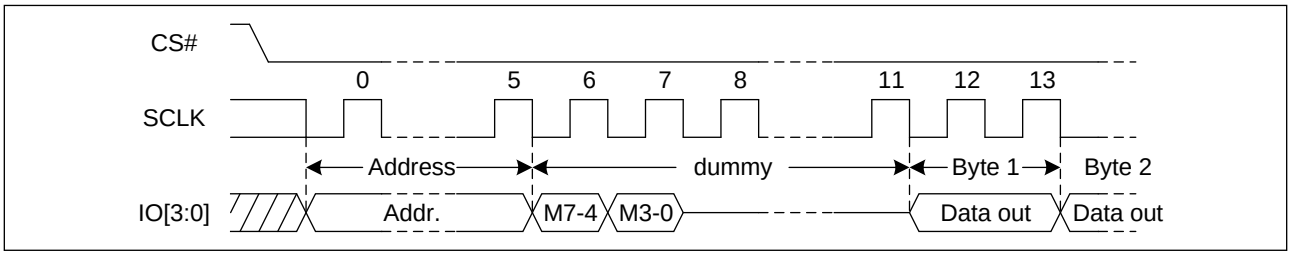
Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

Figure 24. Quad I/O Fast Read Sequence Diagram ((M5-4) ≠ (1, 0), QPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

Figure 25 Quad I/O Fast Read Sequence Diagram ((M5-4) = (1, 0))



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EBH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EBH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

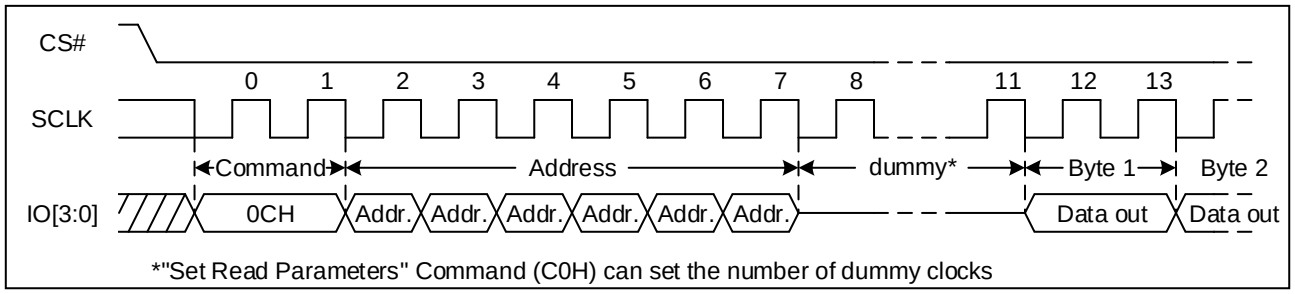
The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap"

command allows three “Wrap Bits” W6-W4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-W5 is used to specify the length of the wrap around section within a page.

7.14 Burst Read with Wrap (0CH)

The “Burst Read with Wrap (0CH)” command provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. This command is similar to the “Fast Read (0BH)” command in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Around” once the ending boundary is reached. The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0H)” command.

Figure 26. Burst Read with Wrap command Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

7.15 Set Burst with Wrap (77H)

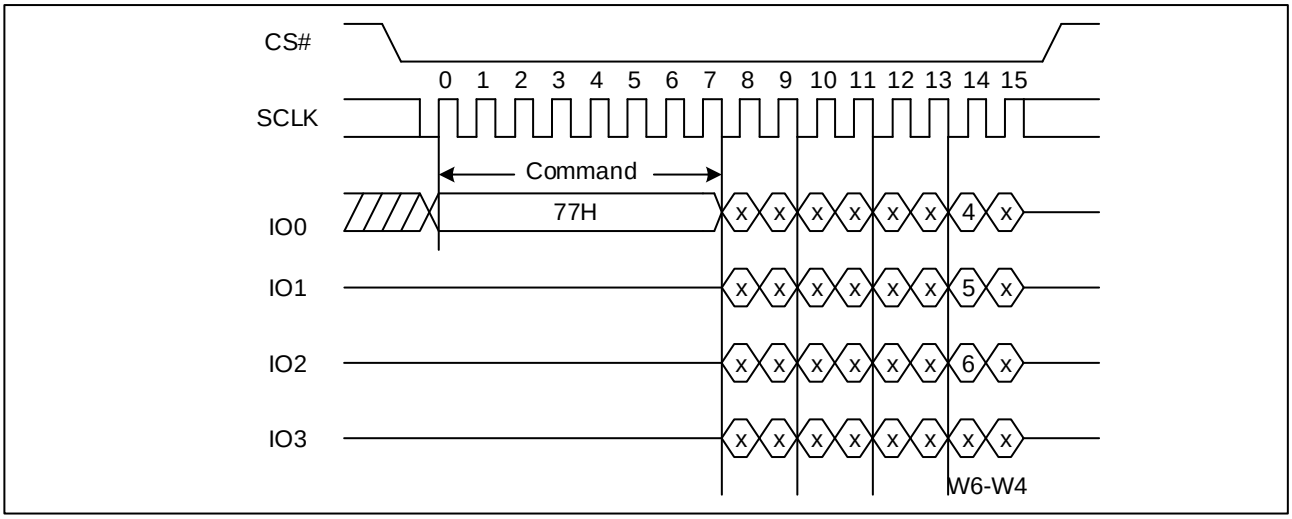
The Set Burst with Wrap command is used in conjunction with “Quad I/O Fast Read” command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits → Send 8 bits “Wrap bits” → CS# goes high.

W6,W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-byte	No	N/A
0, 1	Yes	16-byte	No	N/A
1, 0	Yes	32-byte	No	N/A
1, 1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following “Quad I/O Fast Read” command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

Figure 27. Set Burst with Wrap Sequence Diagram

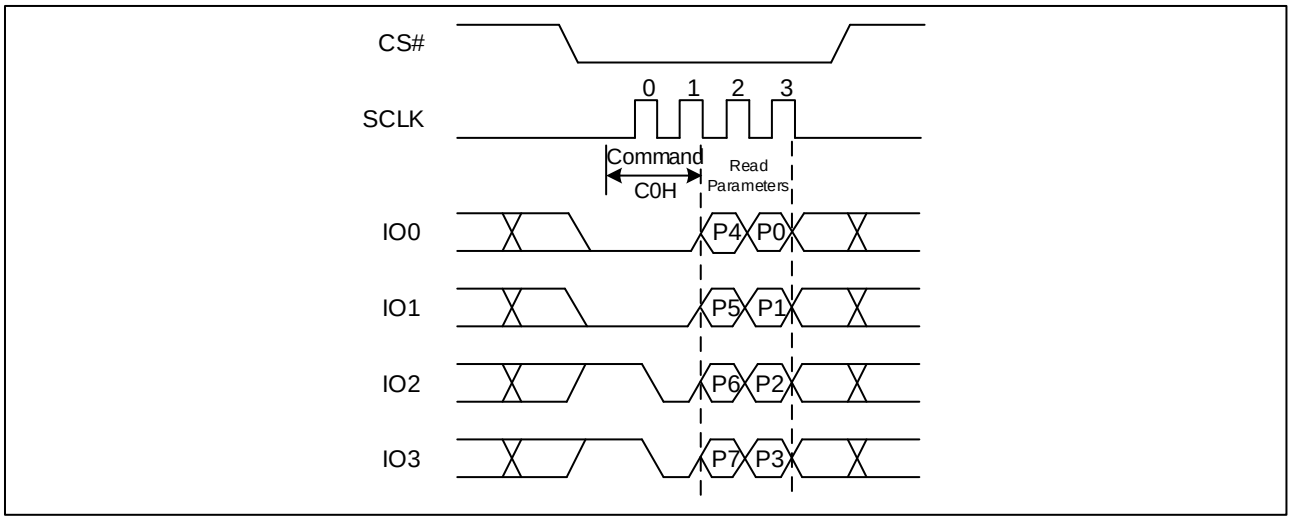


7.16 Set Read Parameters (C0H)

In QPI mode the “Set Read Parameters (C0H)” command can be used to configure the number of dummy clocks for “Fast Read (0BH)”, “Quad I/O Fast Read (EBH)” and “Burst Read with Wrap (0CH)” command, and to configure the number of bytes of “Wrap Length” for the “Burst Read with Wrap (0CH)” command. The “Wrap Length” is set by W5-6 bit in the “Set Burst with Wrap (77H)” command. This wrap setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

P5-P4	Dummy Clocks	Maximum Read Freq.	P1-P0	Wrap Length
0 0	4	80MHz	0 0	8-byte
0 1	6	108MHz	0 1	16-byte
1 0	8	133MHz	1 0	32-byte
1 1	Reserved	Reserved	1 1	64-byte

Figure 28. Set Read Parameters command Sequence Diagram



7.17 Page Program (PP) (02H/12H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously

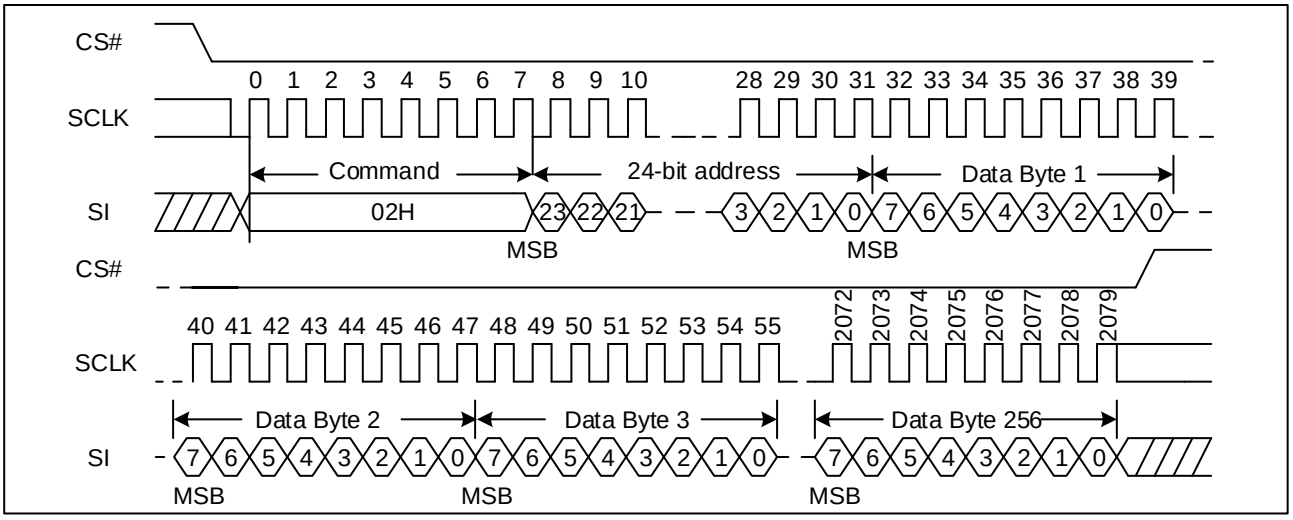
have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3- or 4-Byte address on SI → at least 1 byte data on SI → CS# goes high. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

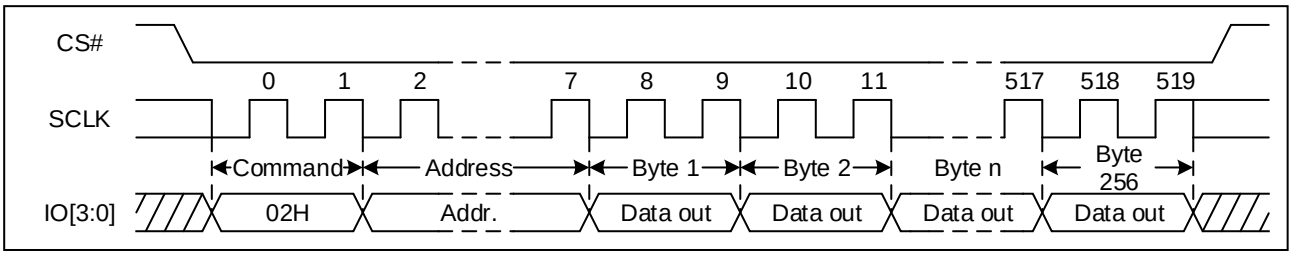
A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 29. Page Program Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

Figure 30. Page Program Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

7.18 Quad Page Program (32H/34H)

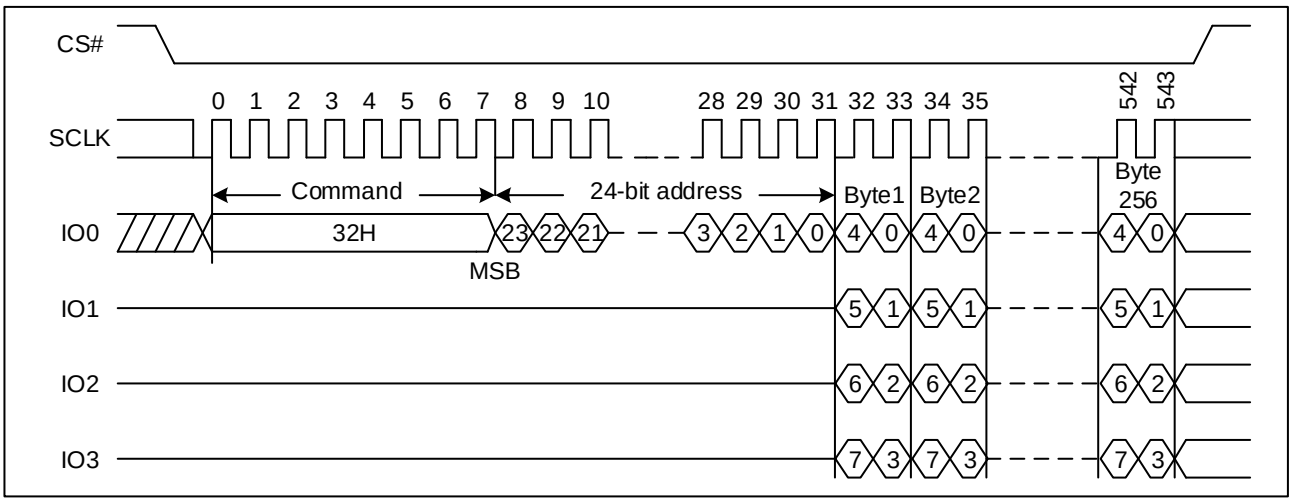
The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address Bytes and at least one data Byte on IO pins.

The command sequence is shown below. If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page. CS# must be driven high after the eighth bit of the last data Byte has been latched in; otherwise the Quad Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is t_{PP}) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 31 Quad Page Program Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

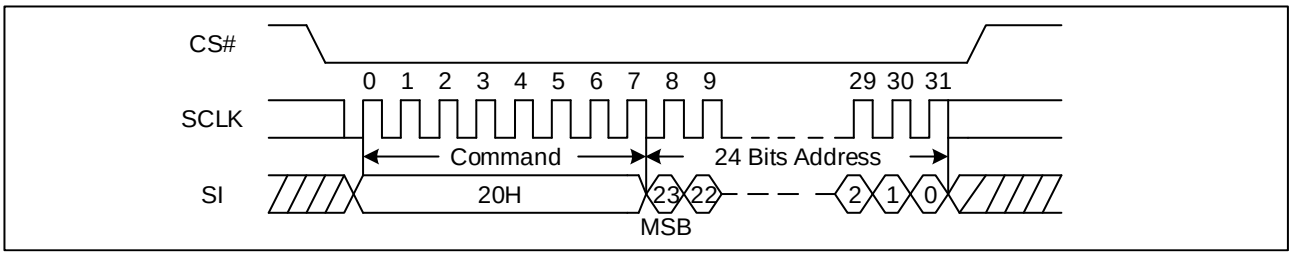
7.19 Sector Erase (SE) (20H/21H)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3- or 4-Byte address on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3- or 4-Byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A

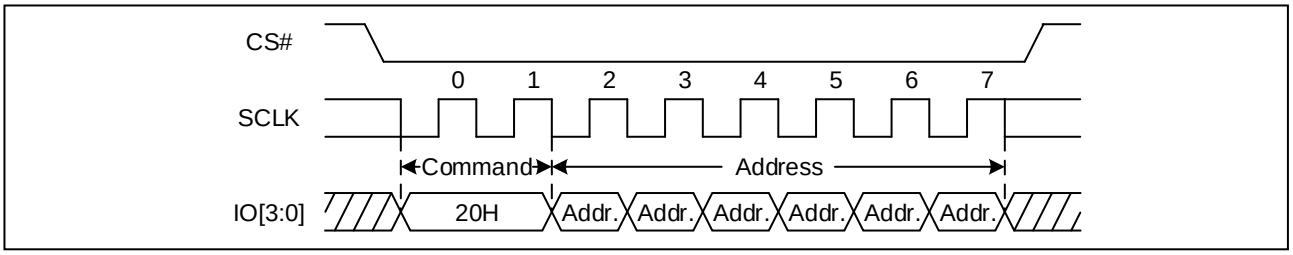
Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bit is not executed.

Figure 32. Sector Erase Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

Figure 33. Sector Erase Sequence Diagram (QPI)



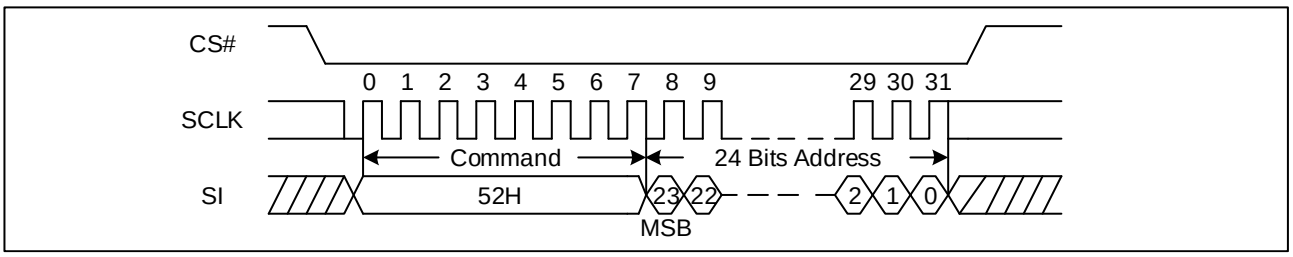
Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

7.20 32KB Block Erase (BE32) (52H/5CH)

The 32KB Block Erase command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase command. CS# must be driven low for the entire duration of the sequence.

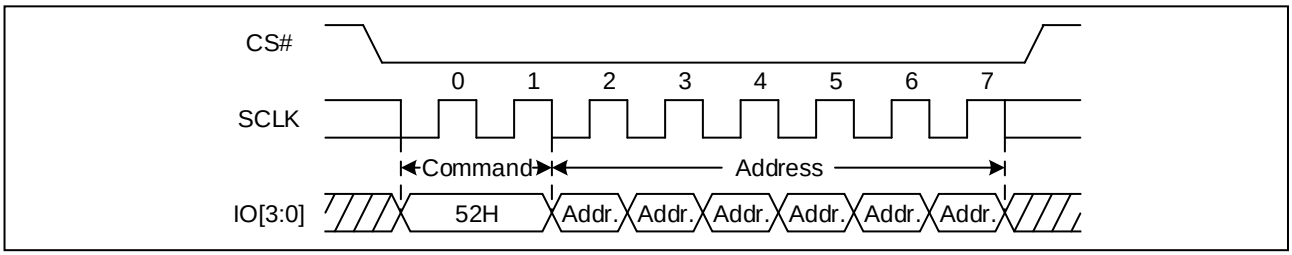
The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3- or 4-Byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE1}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 34. 32KB Block Erase Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

Figure 35. 32KB Block Erase Sequence Diagram (QPI)



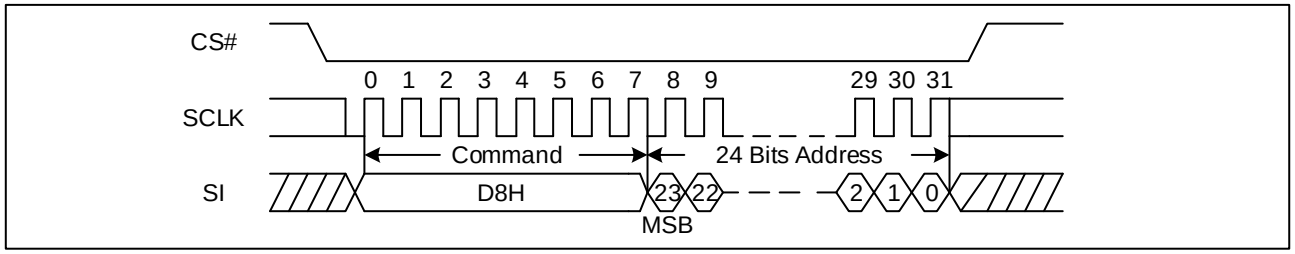
Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

7.21 64KB Block Erase (BE64) (D8H/DCH)

The 64KB Block Erase command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase Command. CS# must be driven low for the entire duration of the sequence.

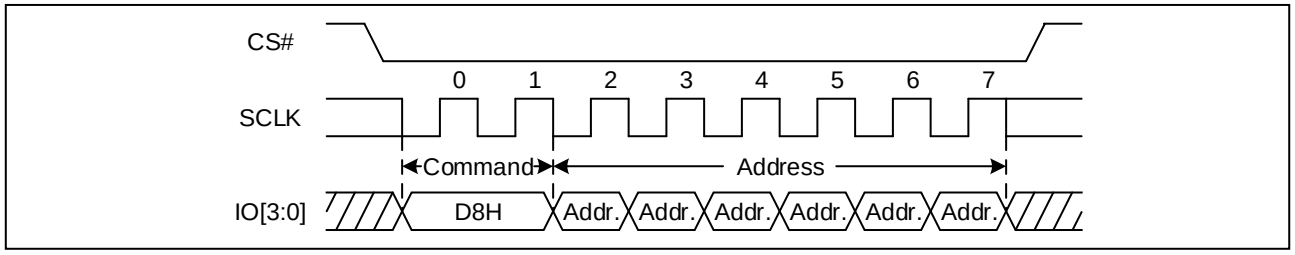
The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-or 4-Byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is t_{BE2}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits is not executed.

Figure 36. 64KB Block Erase Sequence Diagram (SPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

Figure 37. 64KB Block Erase Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

7.22 Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously

have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed, if the no block is protected by the Block Protect bits. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Figure 38. Chip Erase Sequence Diagram (SPI)

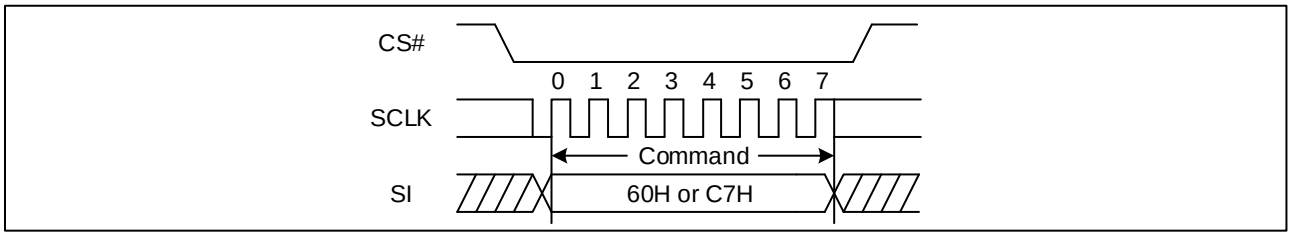
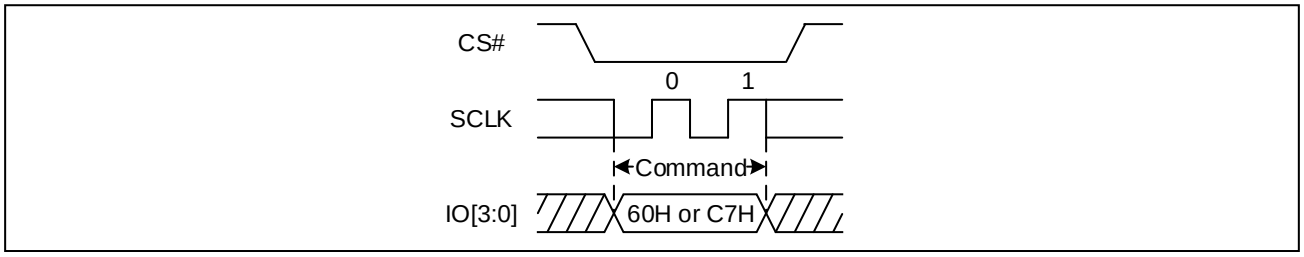


Figure 39. Chip Erase Sequence Diagram (QPI)



7.23 Enter 4-Byte Address Mode (EN4B) (B7H)

The Enter 4-Byte Address Mode command enables accessing the address length of 32-bit for the memory area of higher density (larger than 128Mb). The device default is in 24-bit address mode; after sending out the EN4B instruction, the bit 11 (ADS bit) of status register will be automatically set to "1" to indicate the 4-Byte address mode has been enabled. Once the 4-Byte address mode is enabled, the address length becomes 32-bit instead of the default 24-bit.

All instructions are accepted normally, and just the address bit is changed from 24-bit to 32-bit.

The sequence of issuing EN4B instruction is: CS# goes low → sending Enter 4-Byte mode command →CS# goes high.

Figure 40 Enable 4-Byte Mode Sequence Diagram (SPI)

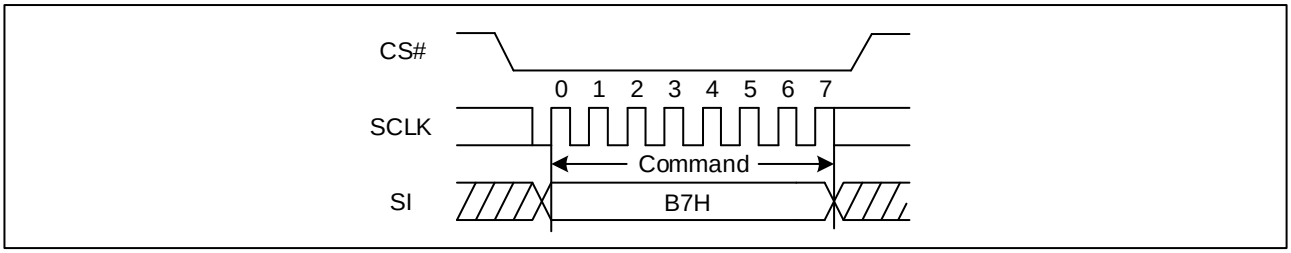
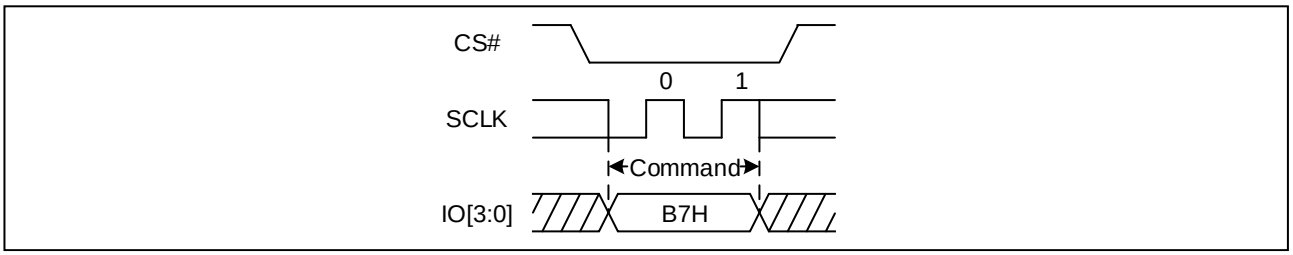


Figure 41 Enable 4-Byte Mode Sequence Diagram (QPI)



7.24 Exit 4-Byte Address Mode (EX4B) (E9H)

The Exit 4-Byte Address Mode command is executed to exit the 4-Byte address mode and return to the default 3-Byte address mode. After sending out the EX4B instruction, the bit 11 (ADS bit) of status register will be cleared to “0” to indicate the exit of the 4-Byte address mode. Once exiting the 4-Byte address mode, the address length will return to 24-bit.

The sequence of issuing EX4B instruction is: CS# goes low → sending Exit 4-Byte Address Mode command →CS# goes high.

Figure 42 Disable 4-Byte Mode Sequence Diagram (SPI)

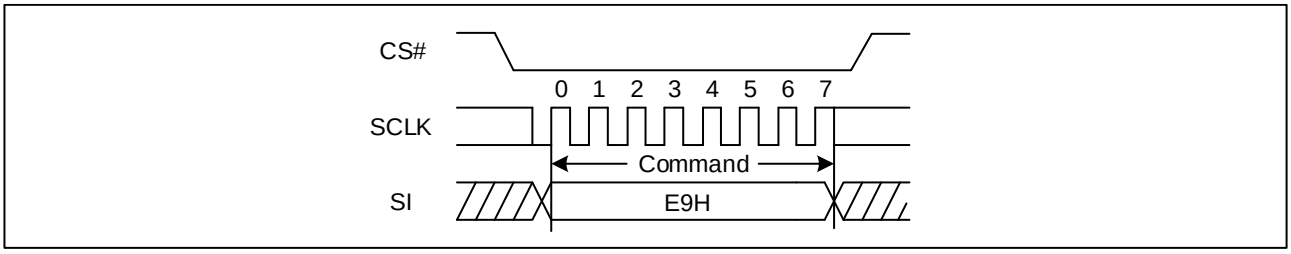
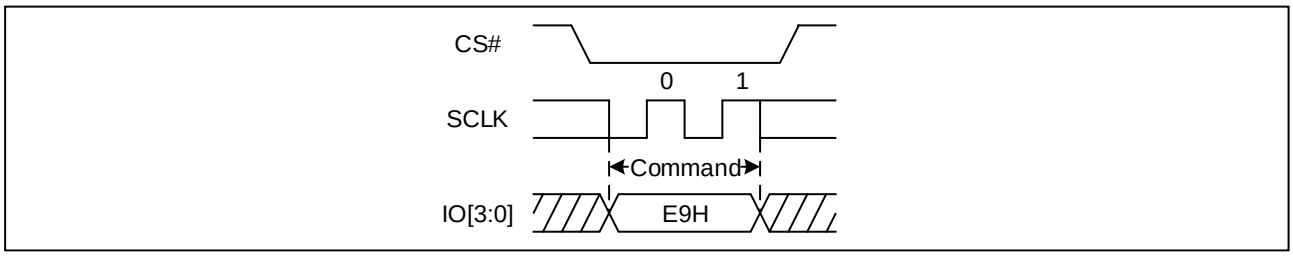


Figure 43 Disable 4-Byte Mode Sequence Diagram (QPI)



7.25 Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first.

Figure 44. Read Manufacture ID/ Device ID Sequence Diagram (SPI)

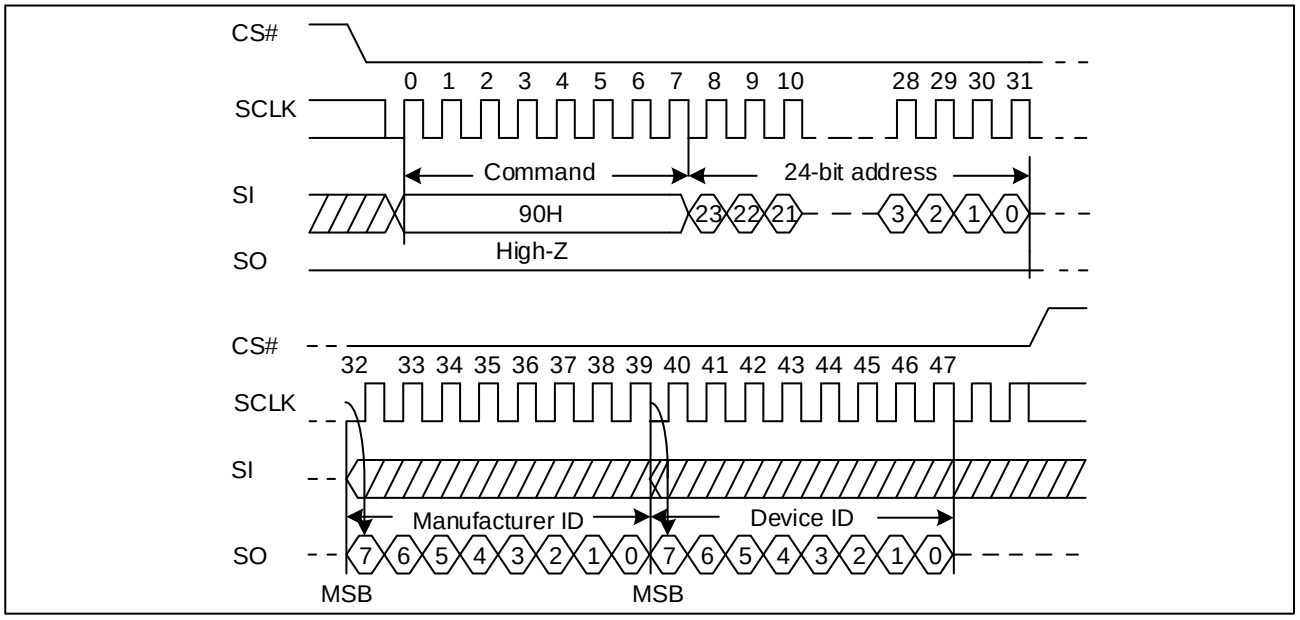
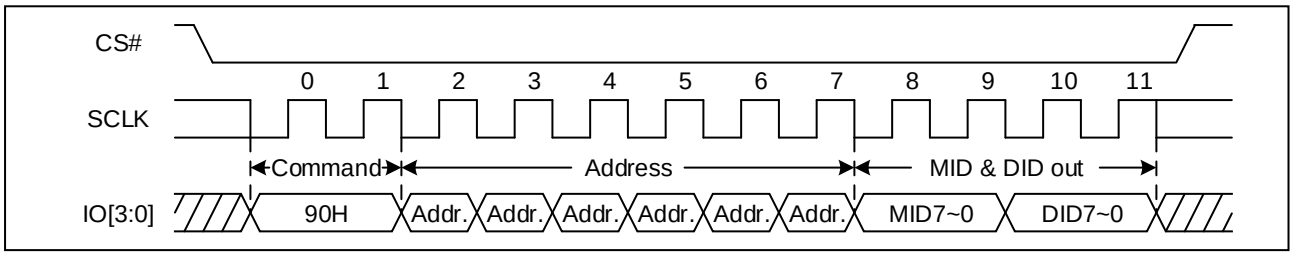


Figure 45. Read Manufacture ID/ Device ID Sequence Diagram (QPI)



7.26 Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory. Each bit is shifted out on the falling edge of Serial Clock. The Read Identification (RDID) command is terminated by driving CS# high at any time during data output. When CS# is driven high, the device is in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 46. Read Identification ID Sequence Diagram (SPI)

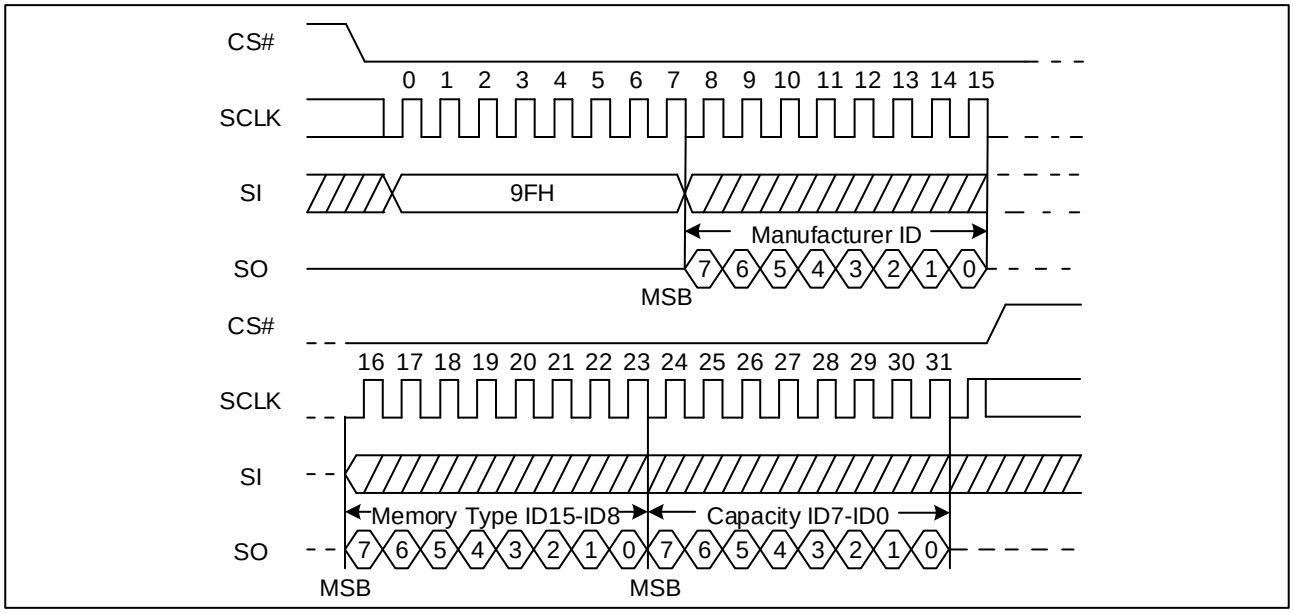
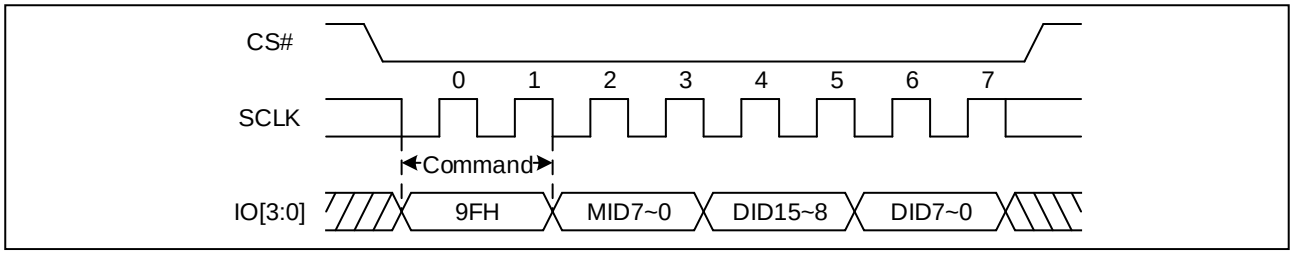


Figure 47. Read Identification ID Sequence Diagram (QPI)

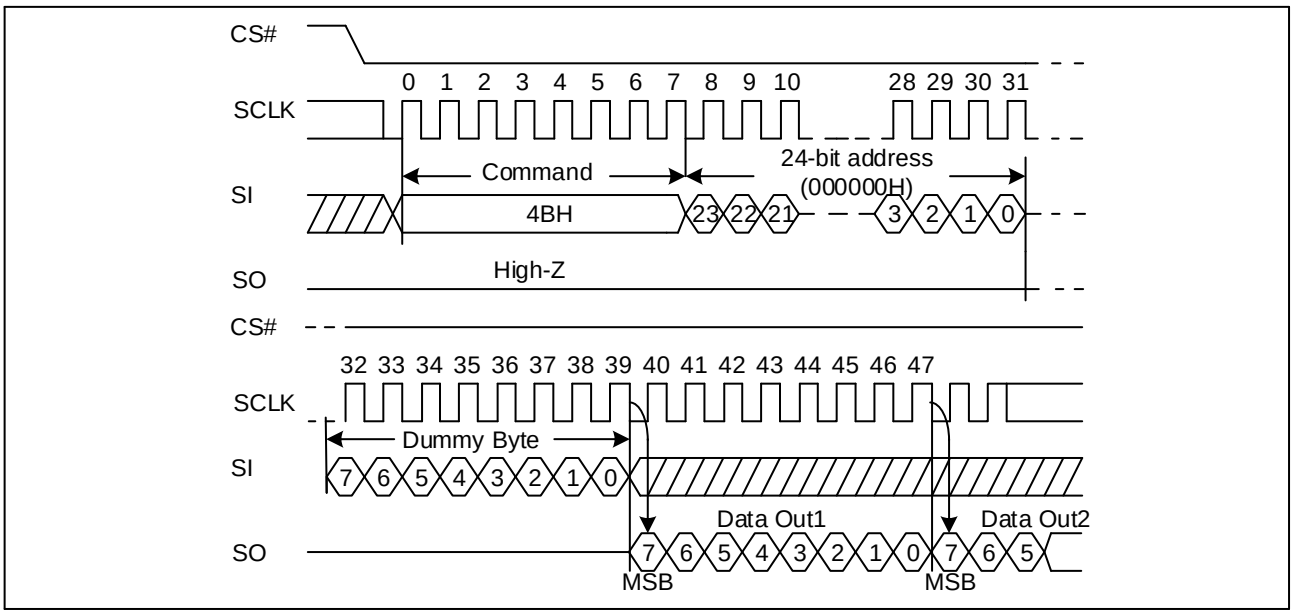


7.27 Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command → 3- or 4-Byte Address (000000H or 00000000H) →Dummy Byte→128bit Unique ID Out →CS# goes high.

Figure 48. Read Unique ID Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

7.28 Erase Security Registers (44H)

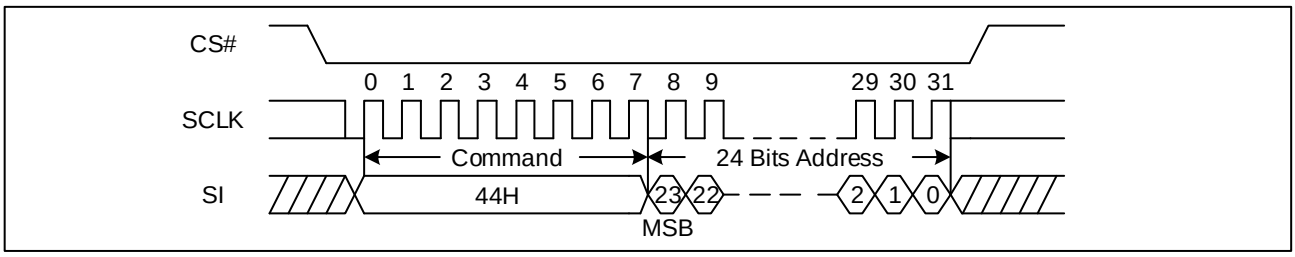
The GD25LQ255E provides 2x1024-Byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → 3- or 4-Byte address on SI → CS# goes high. The command sequence is shown below. CS# must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is t_{SE}) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB2, LB3) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-16	A15-12	A11-10	A9-0
Security Register #2	00H	0010b	00b	Don't care
Security Register #3	00H	0011b	00b	Don't care

Figure 49. Erase Security Registers command Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

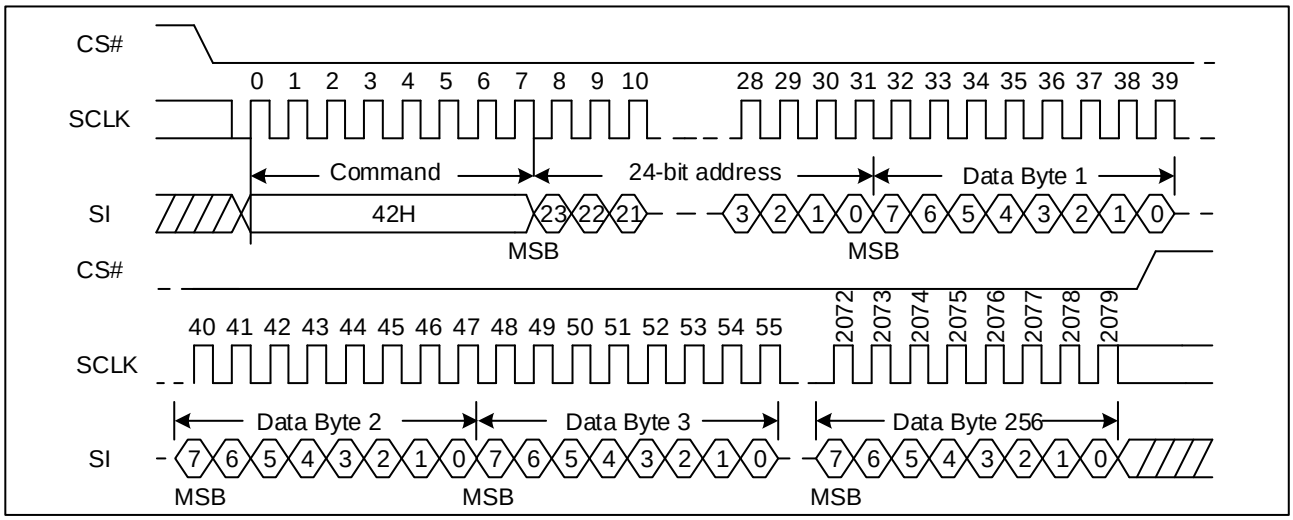
7.29 Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. Each security register contains four pages content. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address Bytes and at least one data Byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is t_{PP}) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB2, LB3) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-16	A15-12	A11-10	A9-0
Security Register #2	00H	0010b	00b	Byte Address
Security Register #3	00H	0011b	00b	Byte Address

Figure 50. Program Security Registers command Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

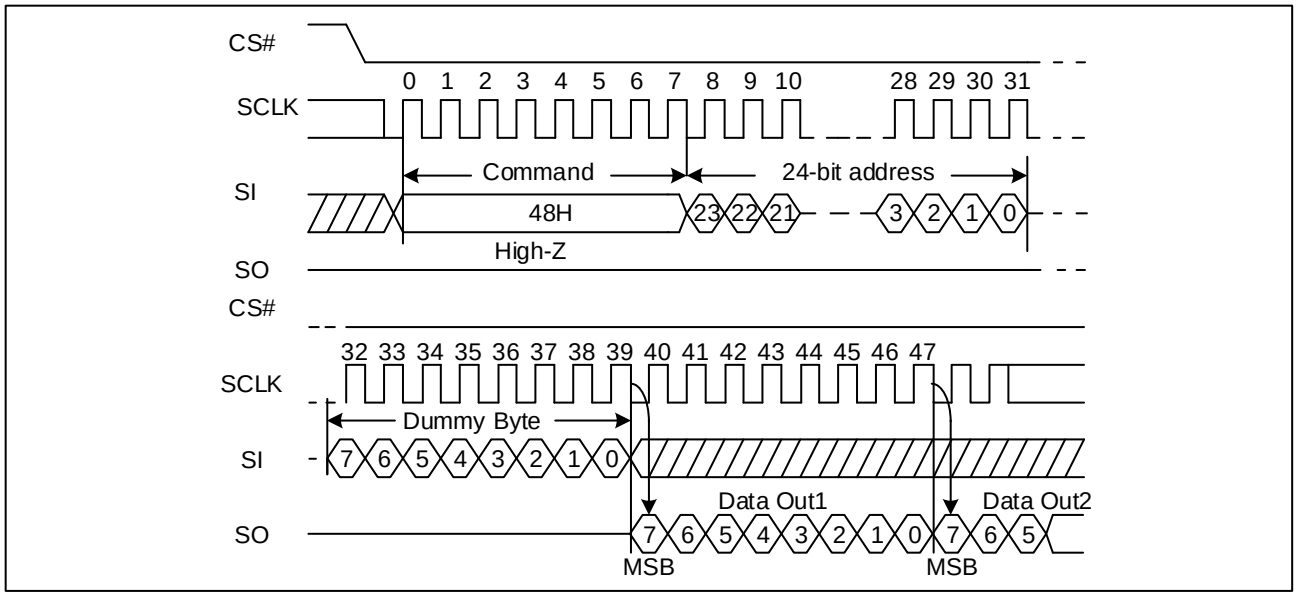
7.30 Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3- or 4-Byte address (A23-A0 or A31-A0) and a dummy Byte, and each bit is latched-in on the rising edge of SCLK. Then the memory

content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency f_C, on the falling edge of SCLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-16	A15-12	A11-10	A9-0
Security Register #2	00H	0010b	00b	Byte Address
Security Register #3	00H	0011b	00b	Byte Address

Figure 51. Read Security Registers command Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-Byte mode or 4-Byte command, the address length is 32-bit.

7.31 Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Read Parameter setting (P7-P0), Deep Power Down Mode, Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4).

The “Enable Reset (66H)” and the “Reset (99H)” commands can be issued in either SPI or QPI mode. The “Enable Reset (66H)” and “Reset (99H)” command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately t_{RST}/t_{RST_E} to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the WIP bit and the SUS1/SUS2 bit in Status Register before issuing the Reset command sequence.

Figure 52. Enable Reset and Reset command Sequence Diagram (SPI)

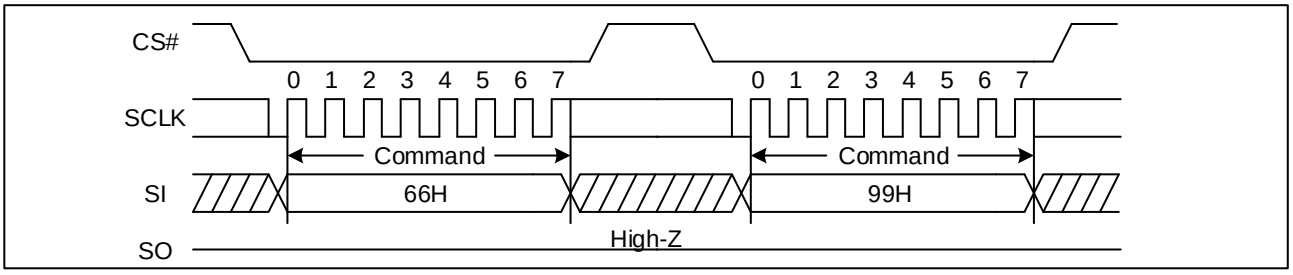
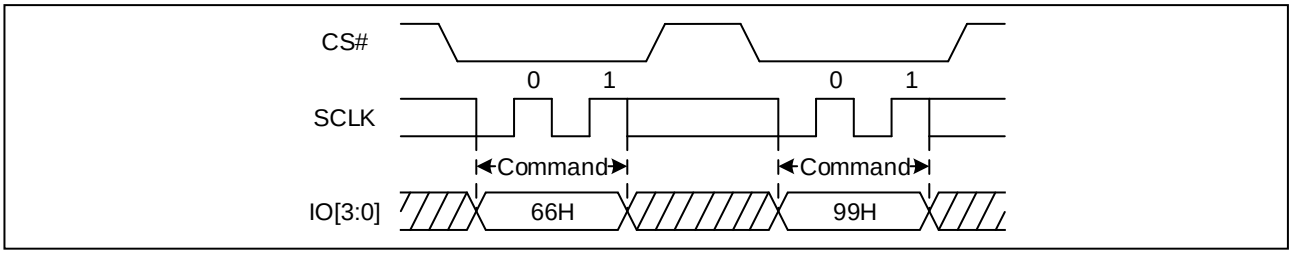


Figure 53. Enable Reset and Reset command Sequence Diagram (QPI)



7.32 Program/Erase Suspend (PES) (75H)

The Program/Erase Suspend command “75H”, allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01H) and Erase/Program Security Registers command (44H, 42H) and Erase commands (20H, 21H, 52H, 5CH, D8H, DCH, C7H, 60H) and Page Program command (02H, 12H, 32H, 34H) are not allowed during Program suspend. The Write Status Register command (01H) and Erase Security Registers command (44H) and Erase commands (20H, 21H, 52H, 5CH, D8H, DCH, C7H, 60H) are not allowed during Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of “tsus” (See AC Characteristics) is required to suspend the program/erase operation.

The Program/Erase Suspend command will be accepted by the device only if the SUS1/SUS2 bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS1/SUS2 bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within “tsus” and the SUS1/SUS2 bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state.

Figure 54. Program/Erase Suspend Sequence Diagram (SPI)

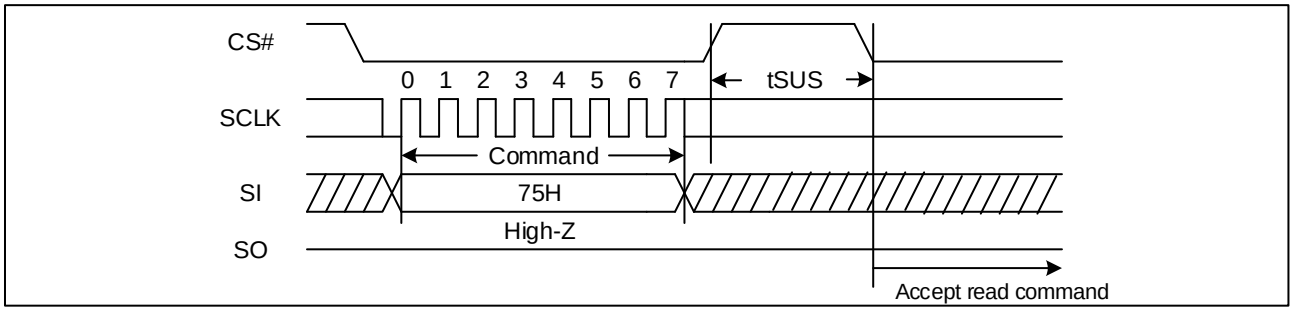
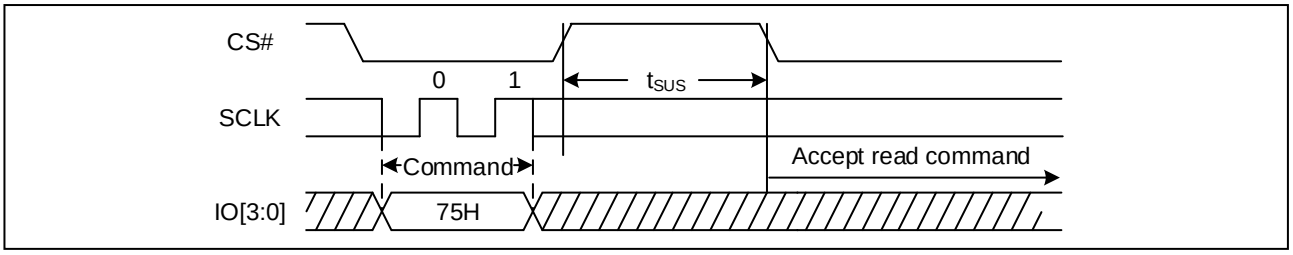


Figure 55. Program/Erase Suspend Sequence Diagram (QPI)



7.33 Program/Erase Resume (PER) (7AH)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase command will be accepted by the device only if the SUS1/SUS2 bit equal to 1 and the WIP bit equal to 0. After issued the SUS1/SUS2 bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active.

Figure 56. Program/Erase Resume Sequence Diagram (SPI)

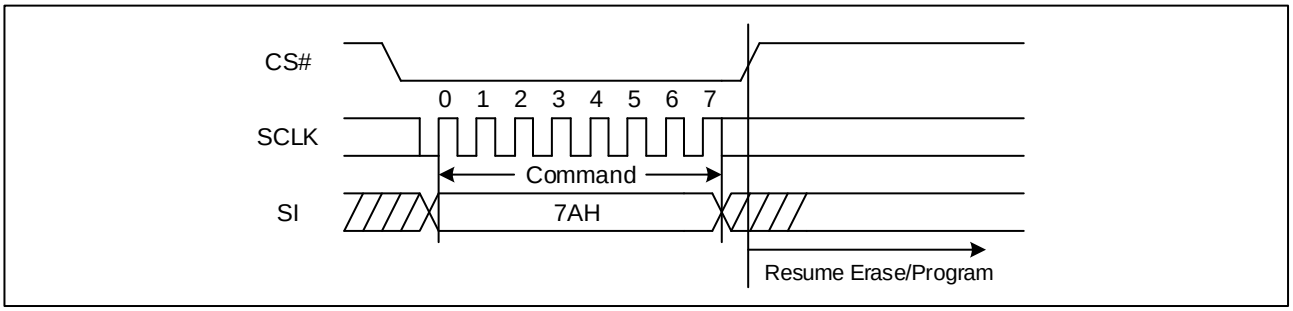
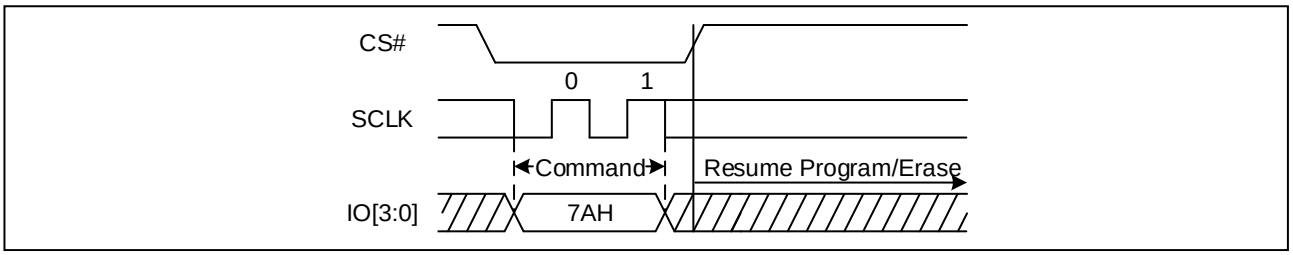


Figure 57. Program/Erase Resume Sequence Diagram (QPI)



7.34 Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command or software reset command. The Release from Deep Power-Down and Read Device ID (RDI) command releases the device from Deep Power-Down mode, also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always in the Standby Mode after Power-Up.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 58. Deep Power-Down Sequence Diagram (SPI)

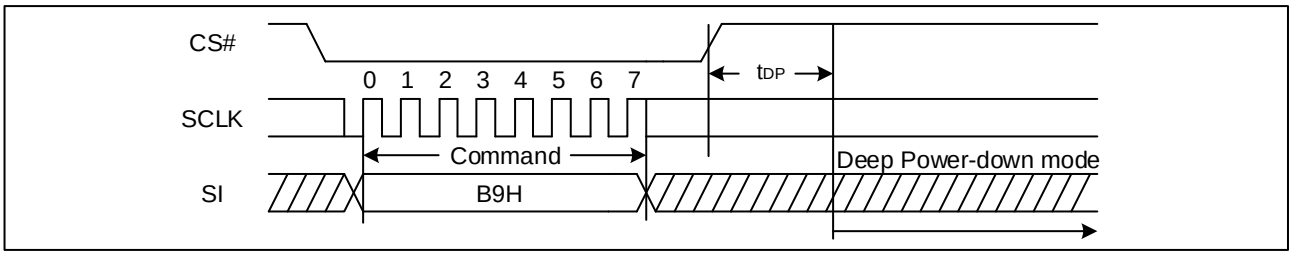
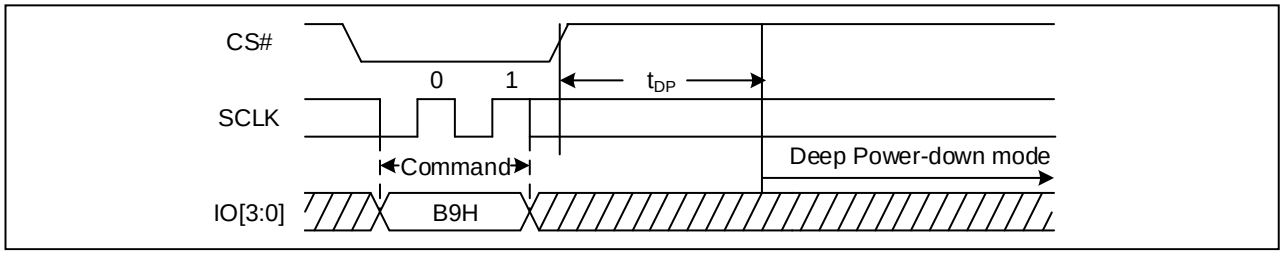


Figure 59. Deep Power-Down Sequence Diagram (QPI)



7.35 Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code "ABH" and driving CS# high. Release from Power-Down will take the time duration of t_{RES1} (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the command is ignored and will not have any effects on the current cycle.

Figure 60. Release Power-Down Sequence Diagram (SPI)

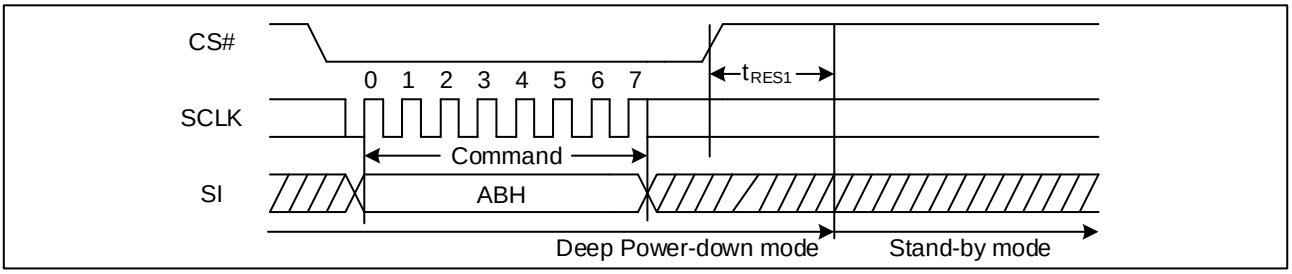


Figure 61. Release Power-Down Sequence Diagram (QPI)

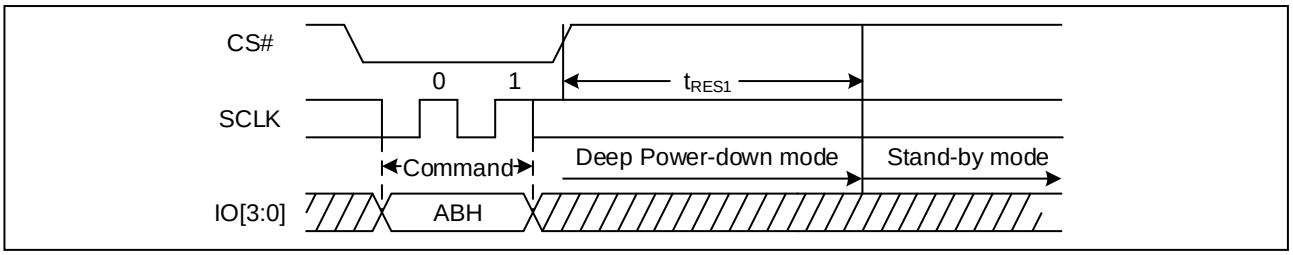


Figure 62. Release Power-Down/Read Device ID Sequence Diagram (SPI)

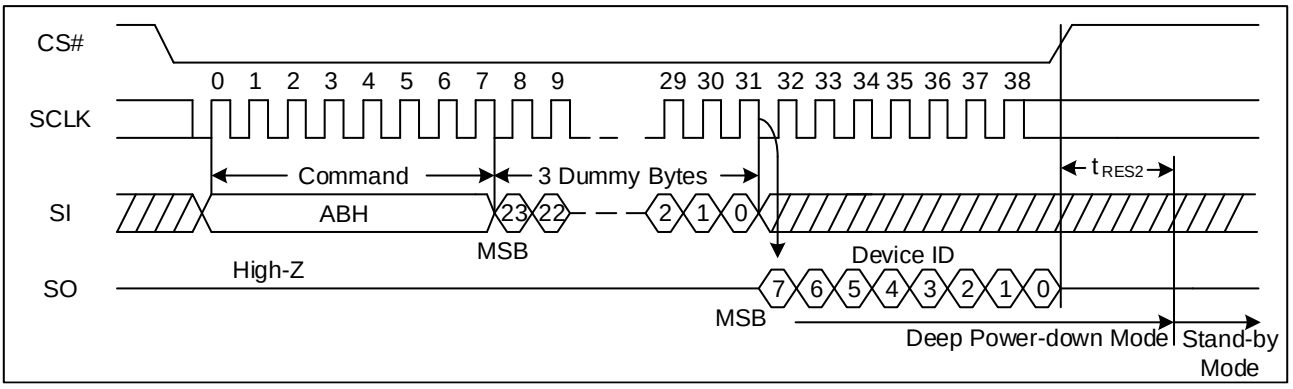
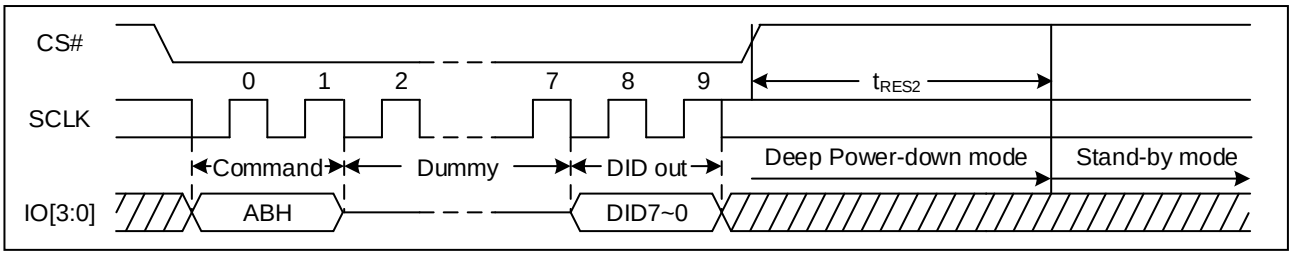


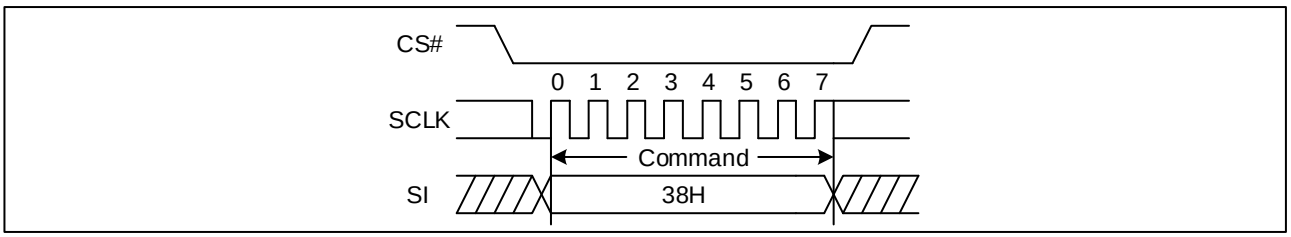
Figure 63. Release Power-Down/Read Device ID Sequence Diagram (QPI)



7.36 Enable QPI (38H)

The GD25LQ255E supports both Standard/Dual/Quad SPI and QPI mode. The “Enable QPI (38H)” command can switch the device from SPI mode to QPI mode. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register must be set to 1 first, and “Enable QPI (38H)” command must be issued. If the QE bit is 0, the “Enable QPI (38H)” command will be ignored and the device will remain in SPI mode. When the device is switched from SPI mode to QPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

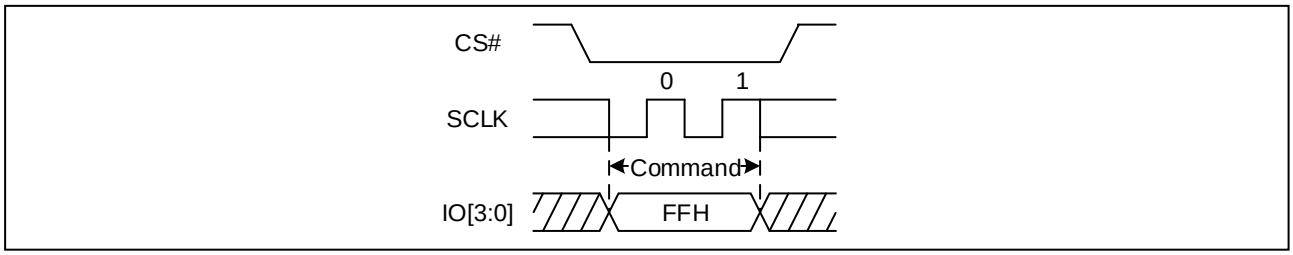
Figure 64. Enable QPI mode command Sequence Diagram



7.37 Disable QPI (FFH)

To exit the QPI mode and return to Standard/Dual/Quad SPI mode, the “Disable QPI (FFH)” command must be issued. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

Figure 65. Disable QPI mode command Sequence Diagram



7.38 Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216B.

Figure 66. Read Serial Flash Discoverable Parameter command Sequence Diagram

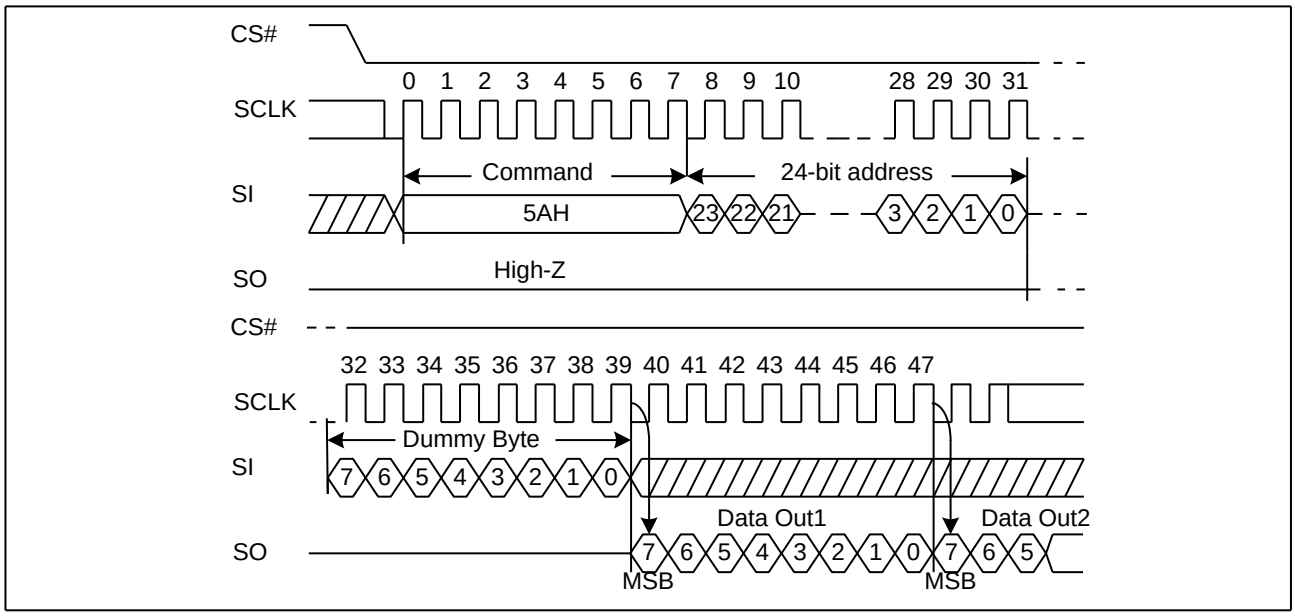


Figure 67. Read Serial Flash Discoverable Parameter command Sequence Diagram (QPI)

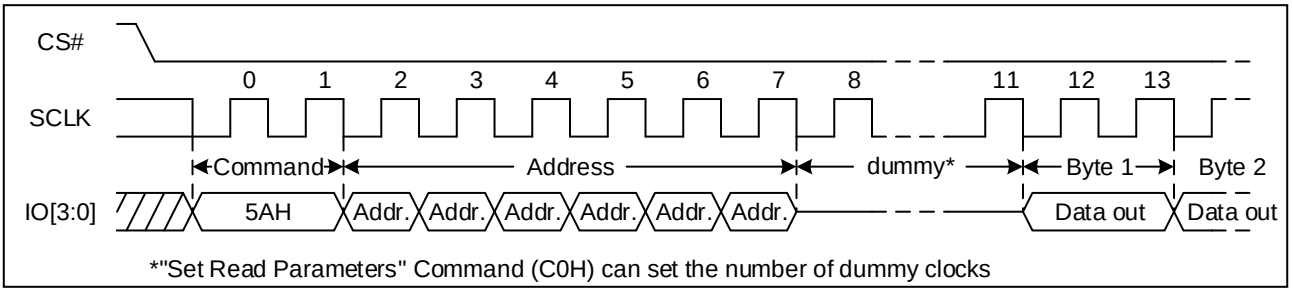


Table 16. Signature and Parameter Identification Data Values (Please contact GigaDevice for Details)

8 ELECTRICAL CHARACTERISTICS

8.1 Power-On Timing

Figure 68. Power-On Timing Sequence Diagram

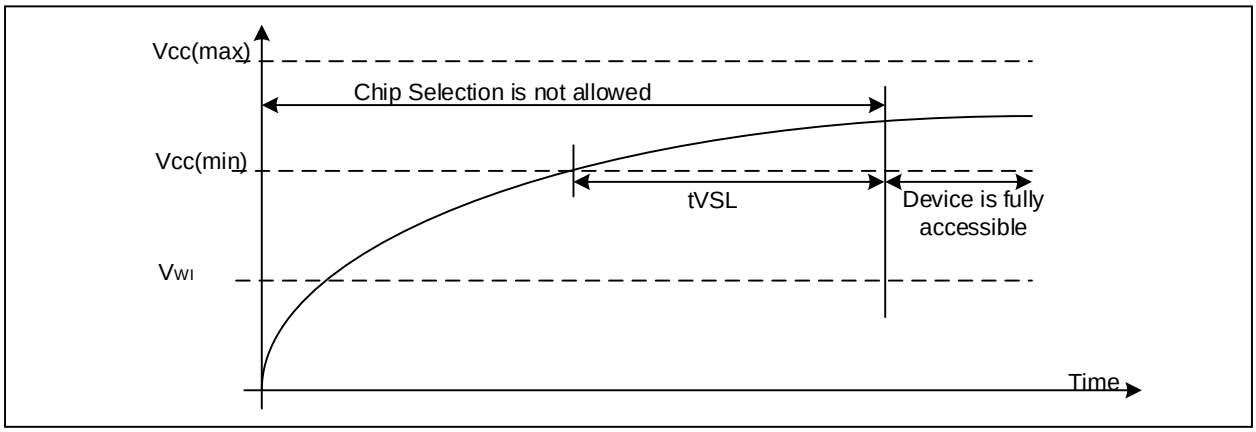


Table 17. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min.) to device operation	1.8		ms
VWI	Write Inhibit Voltage	1	1.5	V

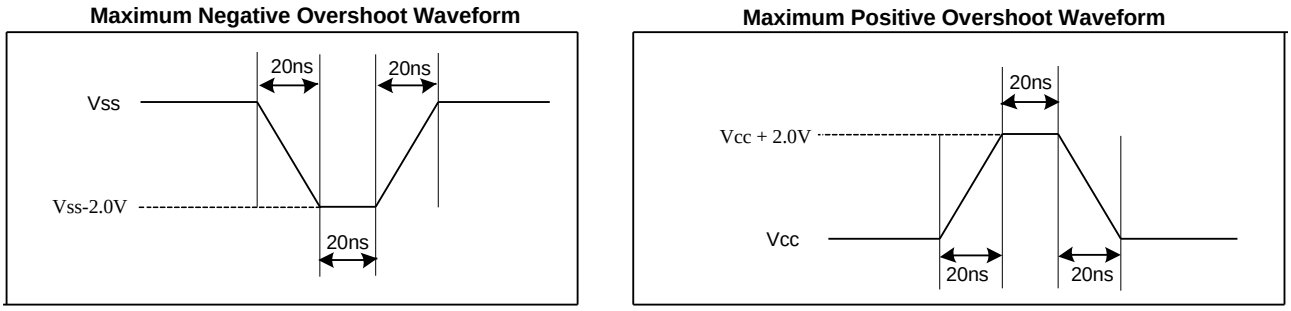
8.2 Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each Byte contains FFH). The Status Register contains 00H (all Status Register bits are 0).

8.3 Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature (T_A)	-40 to 85 -40 to 105 -40 to 125	℃
Storage Temperature	-65 to 150	℃
Transient Input/Output Voltage (note: overshoot)	-2.0 to VCC+2.0	V
Applied Input/Output Voltage	-0.6 to VCC+0.4	V
VCC	-0.6 to 2.5	V

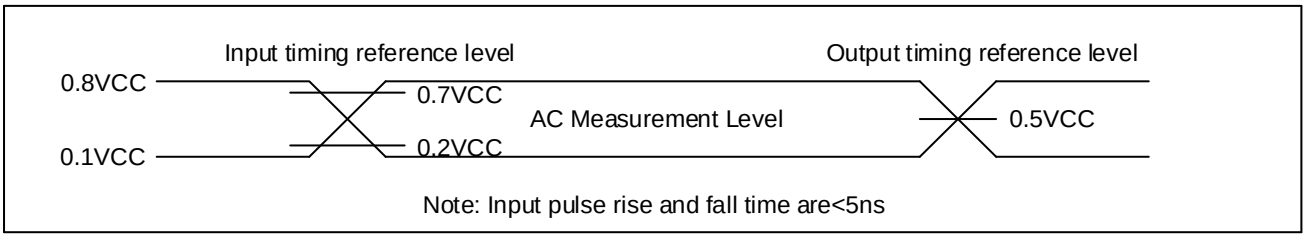
Figure 69. Input Test Waveform and Measurement Level



8.4 Capacitance Measurement Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage		0.1VCC to 0.8VCC		V	
	Input Timing Reference Voltage		0.2VCC to 0.7VCC		V	
	Output Timing Reference Voltage		0.5VCC		V	

Figure 70. Absolute Maximum Ratings Diagram



8.5 DC Characteristics

(T_A = -40℃~85℃, VCC=1.65~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		11	60	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		1	15	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open(x4 I/O)		12	15	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(x4 I/O)		8	12	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		12	20	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		12	20	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		12	20	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		12	20	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		12	20	mA
V_{IL}	Input Low Voltage				0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC			V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Note:

1. Typical value at T_A = 25℃, VCC = 1.8V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

(T_A = -40℃~105℃, VCC=1.65~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		11	120	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		1	50	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open(x4 I/O)		12	15	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(x4 I/O)		8	12	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		12	23	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		12	23	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		12	23	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		12	23	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		12	23	mA
V_{IL}	Input Low Voltage				0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC			V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Note:

1. Typical value at T_A = 25℃, VCC = 1.8V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

(T_A = -40℃~125℃, VCC=1.65~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, VIN=VCC or VSS		11	250	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, VIN=VCC or VSS		1	100	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open(x4 I/O)		12	15	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(x4 I/O)		8	12	mA
I_{CC4}	Operating Current (PP)	CS#=VCC		12	23	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC		12	23	mA
I_{CC6}	Operating Current (SE)	CS#=VCC		12	23	mA
I_{CC7}	Operating Current (BE)	CS#=VCC		12	23	mA
I_{CC8}	Operating Current (CE)	CS#=VCC		12	23	mA
V_{IL}	Input Low Voltage				0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC			V
V_{OL}	Output Low Voltage	I_{OL} = 100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Note:

1. Typical value at T_A = 25℃, VCC = 1.8V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

8.6 AC Characteristics

(T_A = -40℃~85℃, VCC=1.65~2.0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_C	Serial Clock Frequency For: all commands except Read (03H)			133	MHz
f_R	Serial Clock Frequency For: Read (03H)			80	MHz
t_{CLH}	Serial Clock High Time	45% (1/fc_{MAX})			ns
t_{CLL}	Serial Clock Low Time	45% (1/fc_{MAX})			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	1.2			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}	HOLD# Low Setup Time (Relative To Clock)	5			ns
t_{HHCH}	HOLD# High Setup Time (Relative To Clock)	5			ns
t_{CHHH}	HOLD# Low Hold Time (Relative To Clock)	5			ns
t_{CHHL}	HOLD# High Hold Time (Relative To Clock)	5			ns
t_{HLQZ}	HOLD# Low To High-Z Output			6	ns
t_{HHQX}	HOLD# High To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid (CL = 30pF)			7	ns
	Clock Low To Output Valid (CL = 15pF)			6	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			3	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			20	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			20	μs
t_{SUS}	CS# High To Next Command After Suspend			20	μs
t_{RS}	Latency Between Resume And Next Suspend	100			μs
t_{RST}	CS# High To Next Command After Reset (Except From Erase)			30	μs
t_{RST_E}	CS# High To Next Command After Reset (From Erase)			12	ms

t_W	Write Status Register Cycle Time		2	25	ms
t_{BP1}	Byte Program Time (First Byte)		30	60	μs
t_{BP2}	Additional Byte Program Time (After First Byte)		2.5	5	μs
t_{PP}	Page Programming Time		0.25	2.4	ms
t_{SE}	Sector Erase Time		30	300	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.1	0.8	s
t_{BE2}	Block Erase Time (64K Bytes)		0.15	1.2	s
t_{CE}	Chip Erase Time (GD25LQ255E)		64	160	s

Note:

1. Typical value at T_A = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

(T_A = -40℃~105℃, VCC=1.65~2.0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_C	Serial Clock Frequency For: all commands except Read (03H)			133	MHz
f_R	Serial Clock Frequency For: Read (03H)			80	MHz
t_{CLH}	Serial Clock High Time	45% (1/fc_{MAX})			ns
t_{CLL}	Serial Clock Low Time	45% (1/fc_{MAX})			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	1.2			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}	HOLD# Low Setup Time (Relative To Clock)	5			ns
t_{HHCH}	HOLD# High Setup Time (Relative To Clock)	5			ns
t_{CHHH}	HOLD# Low Hold Time (Relative To Clock)	5			ns
t_{CHHL}	HOLD# High Hold Time (Relative To Clock)	5			ns
t_{HLQZ}	HOLD# Low To High-Z Output			6	ns
t_{HHQX}	HOLD# High To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid (CL = 30pF)			7	ns
	Clock Low To Output Valid (CL = 15pF)			6	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			3	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			20	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			20	μs
t_{SUS}	CS# High To Next Command After Suspend			20	μs
t_{RS}	Latency Between Resume And Next Suspend	100			μs
t_{RST}	CS# High To Next Command After Reset (Except From Erase)			30	μs
t_{RST_E}	CS# High To Next Command After Reset (From Erase)			12	ms
t_W	Write Status Register Cycle Time		2	30	ms

t_{BP1}	Byte Program Time (First Byte)		30	60	μs
t_{BP2}	Additional Byte Program Time (After First Byte)		2.5	5	μs
t_{PP}	Page Programming Time		0.25	2.4	ms
t_{SE}	Sector Erase Time		30	400	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.1	1.2	s
t_{BE2}	Block Erase Time (64K Bytes)		0.15	2.4	s
t_{CE}	Chip Erase Time (GD25LQ255E)		64	240	s

Note:

1. Typical value at T_A = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

(T_A = -40℃~125℃, VCC=1.65~2.0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f_C	Serial Clock Frequency For: all commands except Read (03H)			133	MHz
f_R	Serial Clock Frequency For: Read (03H)			80	MHz
t_{CLH}	Serial Clock High Time	45% (1/fc_{MAX})			ns
t_{CLL}	Serial Clock Low Time	45% (1/fc_{MAX})			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	1.2			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}	HOLD# Low Setup Time (Relative To Clock)	5			ns
t_{HHCH}	HOLD# High Setup Time (Relative To Clock)	5			ns
t_{CHHH}	HOLD# Low Hold Time (Relative To Clock)	5			ns
t_{CHHL}	HOLD# High Hold Time (Relative To Clock)	5			ns
t_{HLQZ}	HOLD# Low To High-Z Output			6	ns
t_{HHQX}	HOLD# High To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid (CL = 30pF)			7	ns
	Clock Low To Output Valid (CL = 15pF)			6	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			3	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			20	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			20	μs
t_{SUS}	CS# High To Next Command After Suspend			20	μs
t_{RS}	Latency Between Resume And Next Suspend	100			μs
t_{RST}	CS# High To Next Command After Reset (Except From Erase)			30	μs
t_{RST_E}	CS# High To Next Command After Reset (From Erase)			12	ms
t_W	Write Status Register Cycle Time		2	50	ms

t_{BP1}	Byte Program Time (First Byte)		30	100	μs
t_{BP2}	Additional Byte Program Time (After First Byte)		2.5	10	μs
t_{PP}	Page Programming Time		0.25	4	ms
t_{SE}	Sector Erase Time		30	500	ms
t_{BE1}	Block Erase Time (32K Bytes)		0.1	1.5	s
t_{BE2}	Block Erase Time (64K Bytes)		0.15	3	s
t_{CE}	Chip Erase Time (GD25LQ255E)		64	300	s

Note:

1. Typical value at T_A = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

Figure 71. Input Timing

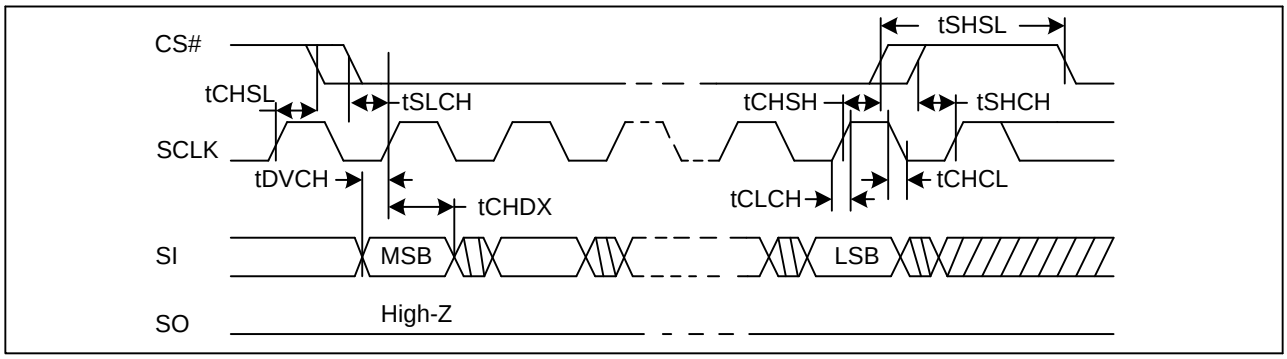


Figure 72. Output Timing

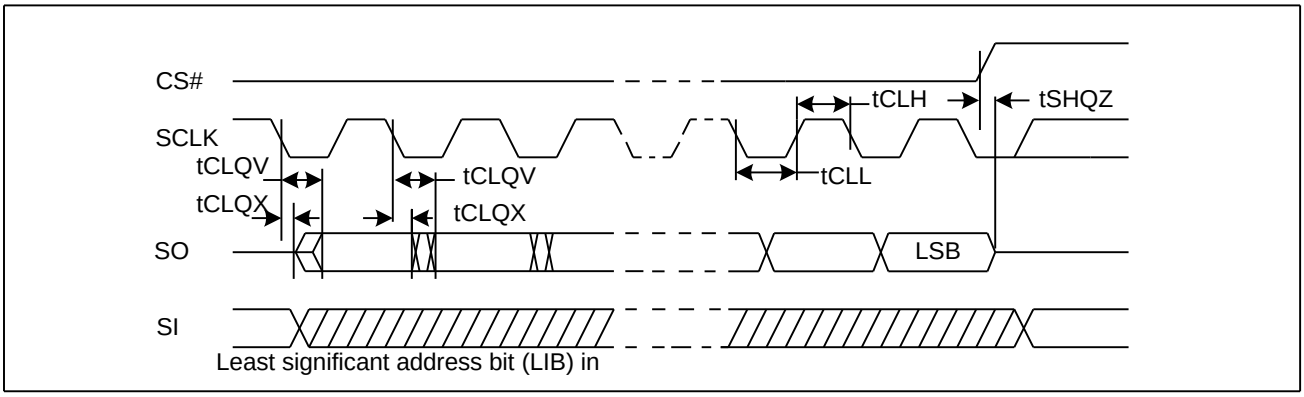


Figure 73. Resume to Suspend Timing Diagram

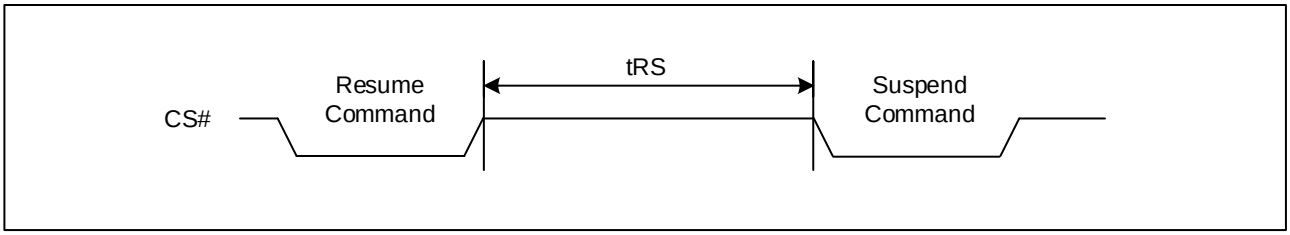


Figure 74. Hold Timing

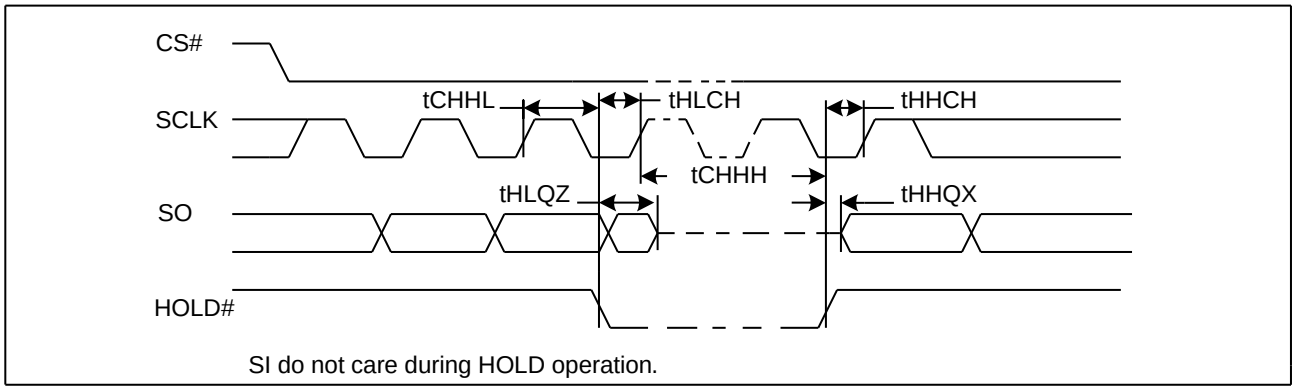


Figure 75 RESET Timing

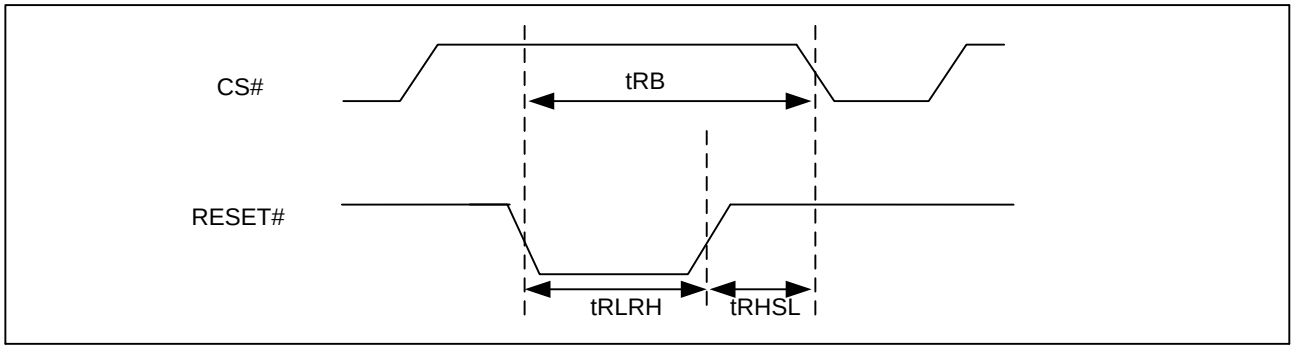


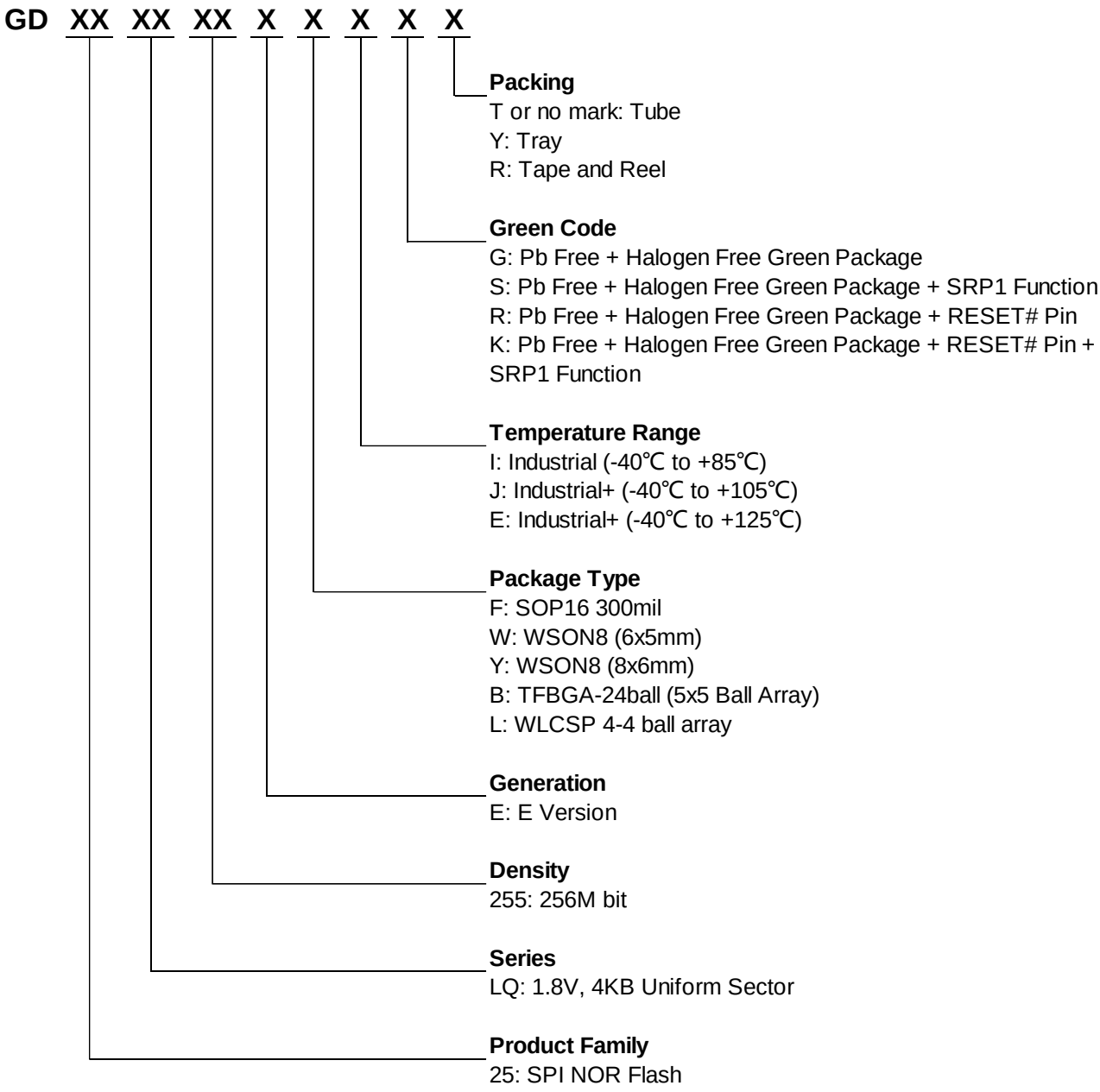
Table 18 Reset Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit.
tRLRH	Reset Pulse Width	1			μs
tRHSL	Reset High Time Before Read	50			ns
tRB	Reset Recovery Time			12	ms

Note:

1. The device need tRB (max) at most to get ready for all commands after RESET# low.

9 ORDERING INFORMATION



9.1 Valid Part Numbers

Please contact GigaDevice regional sales for the latest product selection and available form factors.

Temperature Range I: Industrial (-40℃ to +85℃)

Product Number	Density	Package Type	Packing Options
GD25LQ255EFIR	256Mbit	SOP16 300mil	T/Y/R
GD25LQ255EFIK			
GD25LQ255EWIG	256Mbit	WSON8 (6x5mm)	Y/R
GD25LQ255EWIS			
GD25LQ255EYIG	256Mbit	WSON8 (8x6mm)	Y/R
GD25LQ255EYIS			
GD25LQ255EBIR	256Mbit	TFBGA-24ball (5x5 Ball Array)	Y/R
GD25LQ255EBIK			
GD25LQ255ELIG	256Mbit	WLCSP 4-4 ball array	R
GD25LQ255ELIS			

Temperature Range J: Industrial (-40℃ to +105℃)

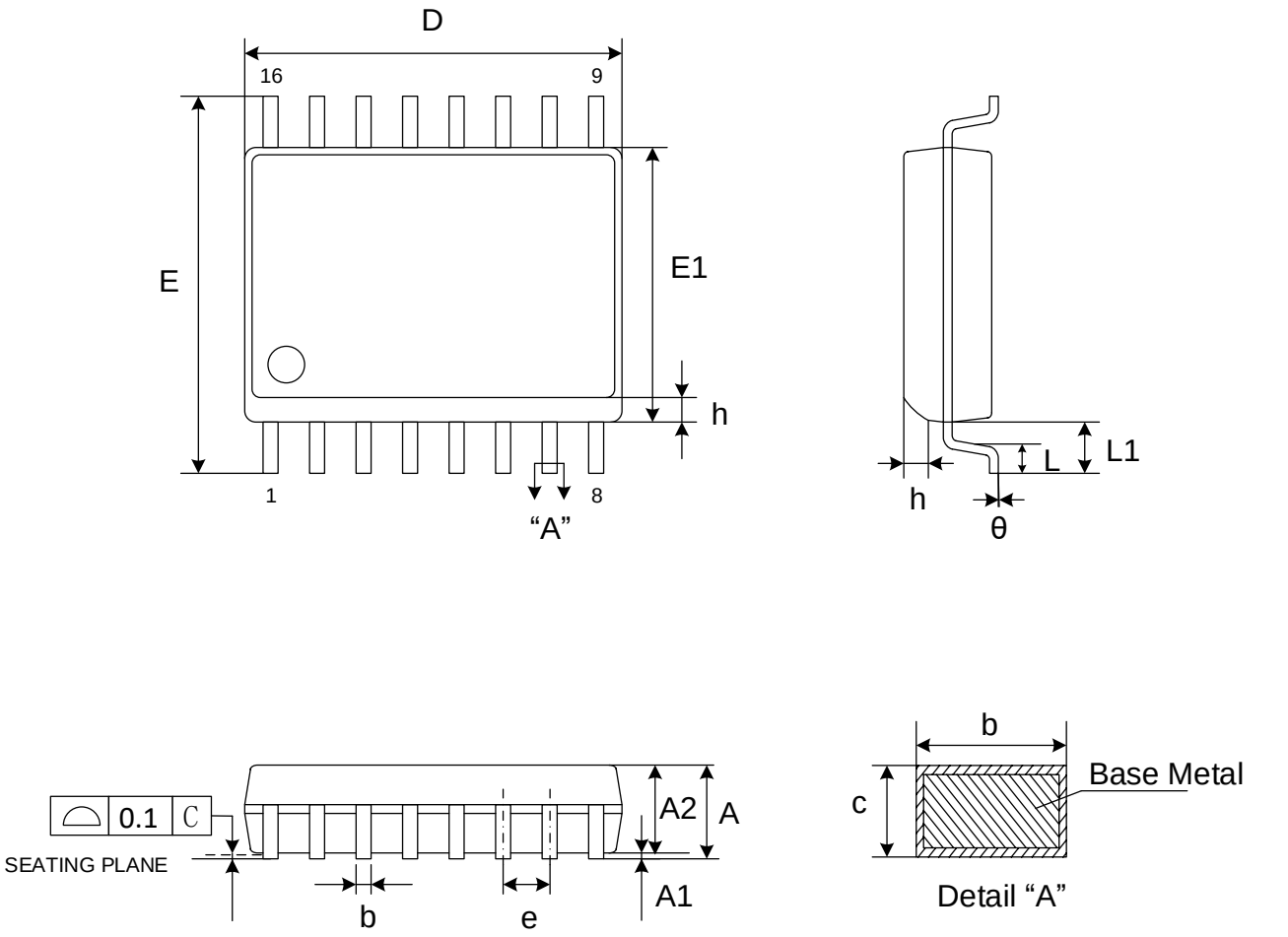
Product Number	Density	Package Type	Packing Options
GD25LQ255EFJR	256Mbit	SOP16 300mil	T/Y/R
GD25LQ255EFJK			
GD25LQ255EWJG	256Mbit	WSON8 (6x5mm)	Y/R
GD25LQ255EWJS			
GD25LQ255EYJG	256Mbit	WSON8 (8x6mm)	Y/R
GD25LQ255EYJS			
GD25LQ255EBJR	256Mbit	TFBGA-24ball (5x5 Ball Array)	Y/R
GD25LQ255EBJK			
GD25LQ255ELJG	256Mbit	WLCSP 4-4 ball array	R
GD25LQ255ELJS			

Temperature Range E: Industrial (-40℃ to +125℃)

Product Number	Density	Package Type	Packing Options
GD25LQ255EFER	256Mbit	SOP16 300mil	T/Y/R
GD25LQ255EFEK			
GD25LQ255EWEG	256Mbit	WSON8 (6x5mm)	Y/R
GD25LQ255EWES			
GD25LQ255EYEG	256Mbit	WSON8 (8x6mm)	Y/R
GD25LQ255EYES			
GD25LQ255EBER	256Mbit	TFBGA-24ball (5x5 Ball Array)	Y/R
GD25LQ255EBEK			
GD25LQ255ELEG	256Mbit	WLCSP 4-4 ball array	R
GD25LQ255ELES			

10 PACKAGE INFORMATION

10.1 Package SOP16 300MIL



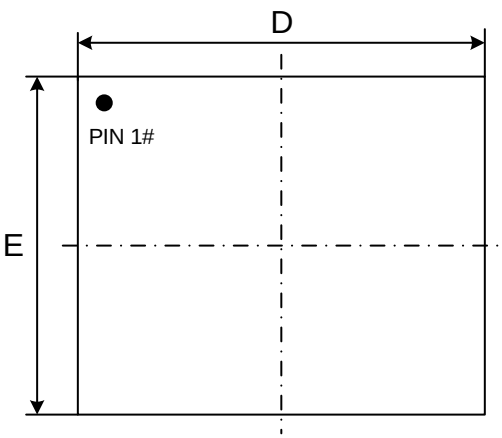
Dimensions

Symbol		A	A1	A2	b	c	D	E	E1	e	L	L1	h	θ
Unit														
mm	Min	-	0.10	2.05	0.31	0.10	10.20	10.10	7.40	1.27	0.40	1.40	0.25	0
	Nom	-	0.20	-	0.41	0.25	10.30	10.30	7.50		-		-	-
	Max	2.65	0.30	2.55	0.51	0.33	10.40	10.50	7.60		1.27		0.75	8

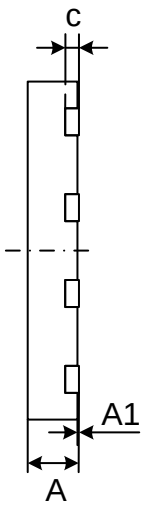
Note:

1. Both the package length and width do not include the mold flash.

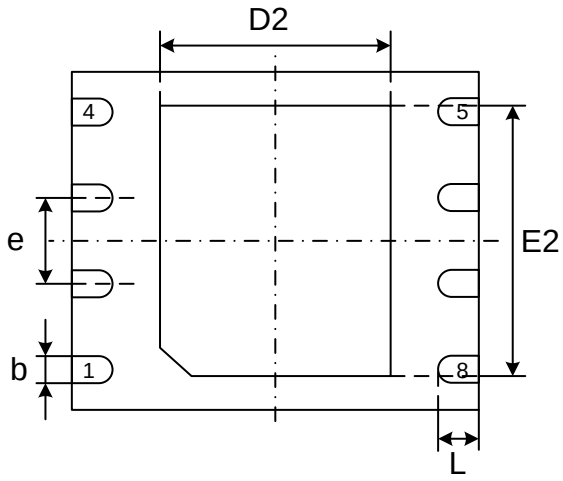
10.2 Package WSON8 (6x5mm)



Top View



Side View



Bottom View

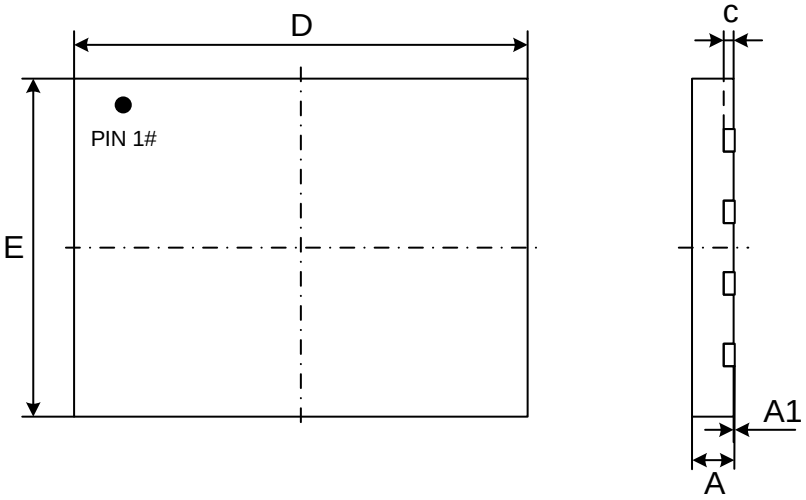
Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	5.90	3.30	4.90	3.90	1.27	0.50
	Nom	0.75	0.02	0.203	0.40	6.00	3.40	5.00	4.00		0.60
	Max	0.80	0.05	0.250	0.50	6.10	3.50	5.10	4.10		0.75

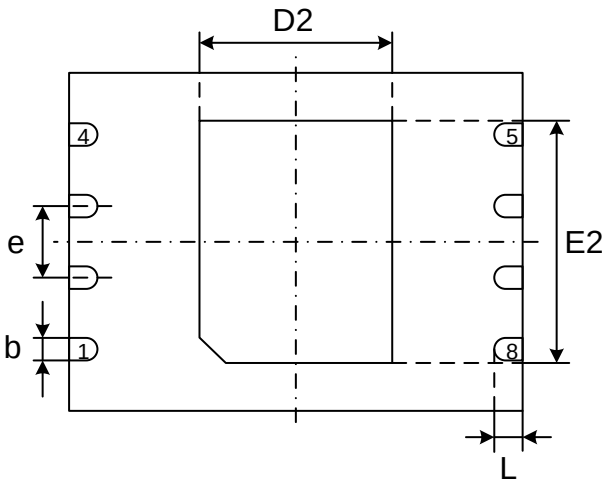
Note:

1. The exposed metal pad area on the bottom of the package is floating.
2. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
3. The lead shape may be of little difference according to different package lead frames. These lead shapes are compatible with each other.

10.3 Package WSON8 (8x6mm)



Top View Side View



Bottom View

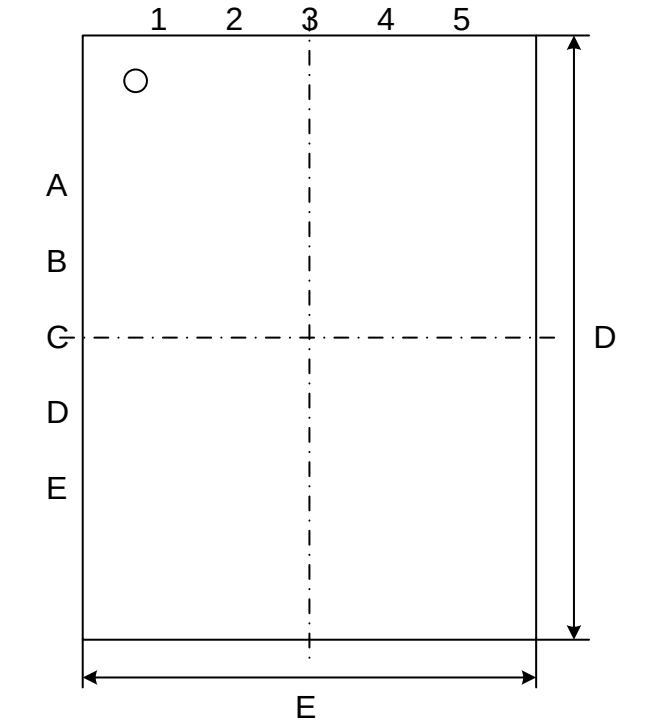
Dimensions

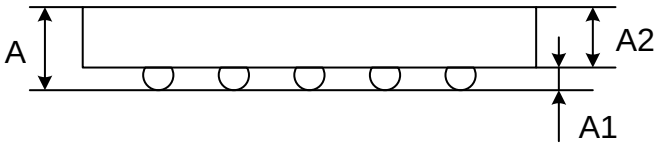
Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.10	4.40		0.55

Note:

1. The exposed metal pad area on the bottom of the package is floating.
2. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
3. The lead shape may be of little difference according to different package lead frames. These lead shapes are compatible with each other.

10.4 Package TFBGA-24BALL (5x5 ball array)

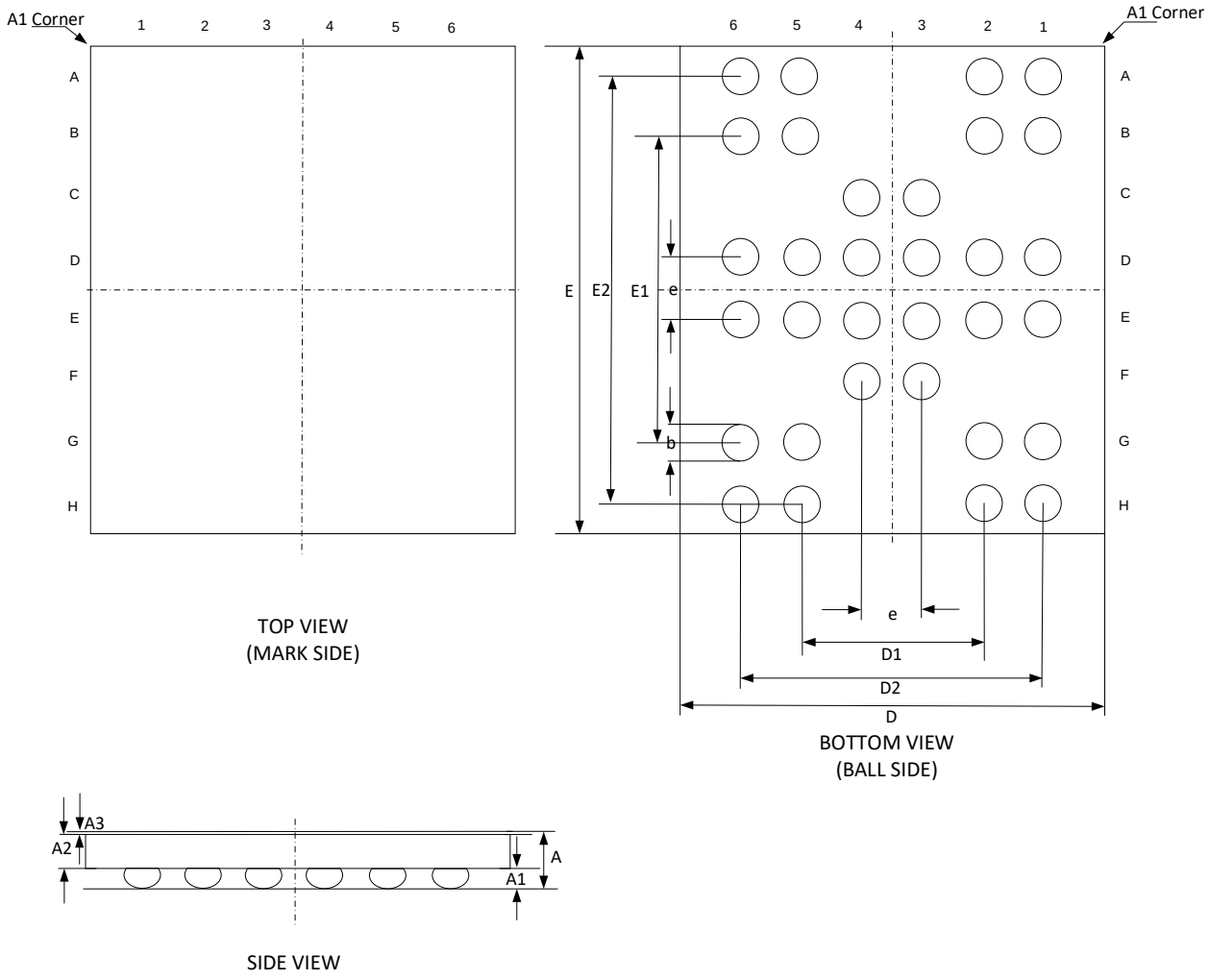




Dimensions

Symbol / Unit		A	A1	A2	b	E	E1	D	D1	e
mm	Min	-	0.25	-	0.35	5.90	4.00	7.90	4.00	1.00
	Nom	-	0.30	0.80	0.40	6.00		8.00		
	Max	1.20	0.35	-	0.45	6.10		8.10		

10.5 Package WLCSP 4-4 ball array



Dimensions

Symbol / Unit		A	A1	A2	A3	b	D1	D2	E1	E2	e
mm	Min	0.440	0.145	0.265	0.025 BSC	0.270	1.500 BSC	2.500 BSC	2.500 BSC	3.500 BSC	0.500 BSC
	Nom	0.470	0.165	0.285		0.300					
	Max	0.500	0.185	0.305		0.330					

Note:

1. Please contact GigaDevice for full dimension information

11 REVISION HISTORY

Version No	Description	Page	Date
1.0	Initial release	All	2020-9-16
1.1	Modify Dummy Clock Typo of Figure 25	P34	2022-11-28
	Update Ordering Information	P66-68	
	Add Coplanarity of SOP16	P69	
	Modify TFBGA-24Ball Dimensions Table	P72	
	Modify POD of WLCSP 4-4 Ball Array Package	P73	
1.2	Modify Dimensions of WLCSP 4-4 Ball Array Package	P73	2024-7-4

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