GigaDevice Semiconductor Inc.

GD30DR830x
3-Phase Motor Driver

Datasheet

Table of Contents

List of Figures

List of Tables

1. Features

- 4.5V to 30V Supply Voltage
- Programmable gate drive current, peak 1A source and 1.2A sink current of GD30DR830x
- Smart high-side and low-side Slew-Rate Control
- PWM input control up to 200kHz
- Only supported 6 PWM mode
- Inside 5V/2A DC-DC buck controller(GD30DR8306x Only)
- 3.3V and 5V digital interface
- Integrated 5V LDO
- Thermally-Enhanced: GD30DR8306x QFN32(5x5), GD30DR8304x QFN24(4X4)
- Protection Features:
  - Dead time insertion
  - MOSFET Shoot Through protection
  - Over temperature protection
  - Fault diagnostics
  - VP and VDD Under Voltage Lock-Out(UVLO)

2. Applications

- 3-Phase BLDC and PMSM Motors
- Power Tools
- Robotics and RC Toys
- Industrial Automation

3. General description

The versatile programmable features listed below allow GD30DR830x to be used in a broad range of applications, such as 3-phase BLDC motors, electronic bikes, power tools, and etc.

The GD30DR830x is a three-phase gate driver IC integrated with an optional DC/DC buck controller(GD30DR8306x only). The IC includes three half-bridge drivers, each is capable of driving two NMOSFETs and supports up to 1A source and 1.2A sink current capability. The drive currents will be adapted automatically to the optimized current according to different power MOSFET used in the application. A proprietary slew rate control is implemented to reduce the EMI of gate drive. The GD30DR830x can operate with a single power supply ranging from 4.5V to 30V. A regulated charge pump supporting 100% duty cycle is integrated in the device to supply the gate drive current and the internal LDOs.

The device inserts fixed dead-time and uses automatic handshaking to prevent the high-side and low-side MOSFET from shoot-through when switching.

The optional integrated DC/DC buck controller operates with power supply of 4.5V to 30V and the output voltage is 5V. The driver can drive an external NMOSFET up to 2A.

The versatile programmable features of the IC allow for it to be used in a broad range of applications, such as 3-phase BLDC motors, electronic bikes, power tools, and etc.

The GD30DR8306x is available in thermal enhanced package QFN32(5X5) with buck controller. The GD30DR8304x is available in thermal enhanced package QFN24(4X4) without buck controller.

4. Device overview

4.1. Device Comparison Table

Table 4-1. Device conparison infromation for GD30DR830x

Code	Package	PWM Mode	Gate driver Current	Buck(V)
GD30DR8306x	QFN32(5X5)	6 PWM	Hardware configurable Default 1.0A source/1.2A sink	5V
GD30DR8304x	QFN24(4X4)	6 PWM	Fixed 500mA source/600mA sink	None

4.2. Block diagram

Figure 4-1. Block diagram for GD30DR8306x

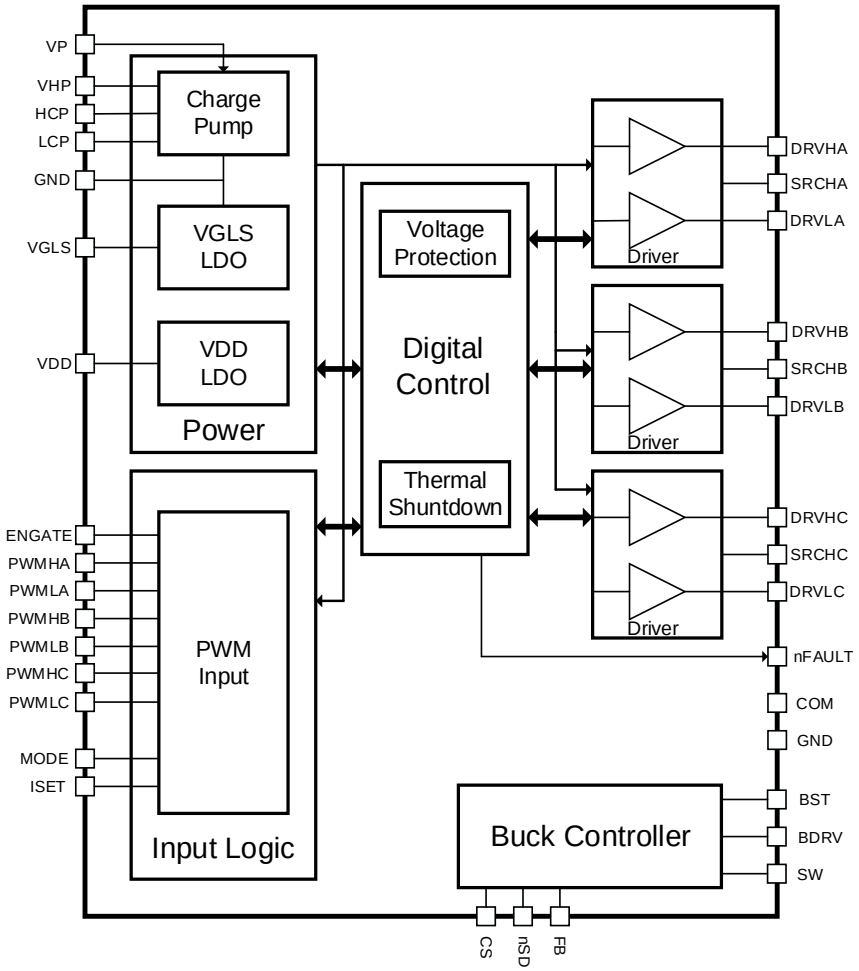
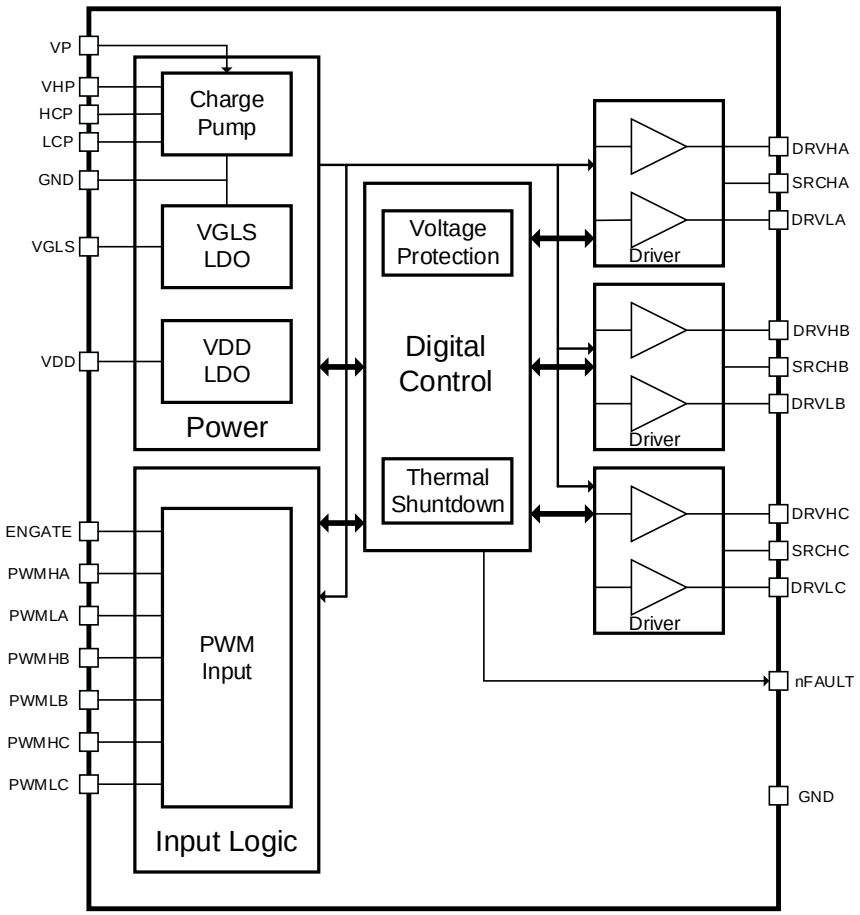


Figure 4-2. Block diagram for GD30DR8304x



4.3. Pinout and pin assignment

Figure 4-3. GD30DR8306x QFN32 pinouts

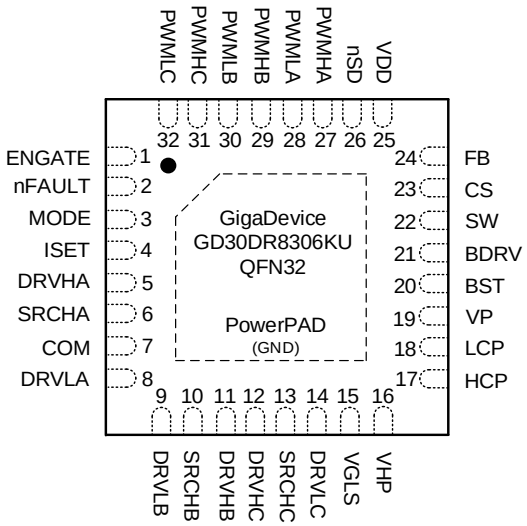
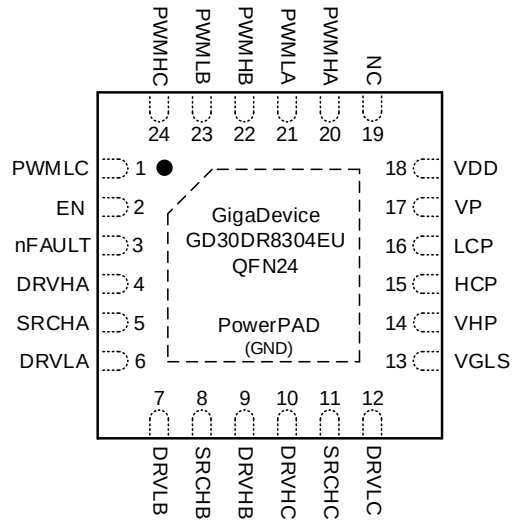


Figure 4-4. GD30DR8304x QFN24 pinouts



4.4. Pin definitions

The table below shows the pin definition of GD30DR8306x.

Table 4-2. GD30DR8306x pin configuration

Pin Name	Pins	Pin Type	Functions Description	
ENGATE	1	I	Enable gate driver	Enables the gate driver, internal pull-down.
nFAULT	2	OD	Fault indicator	The low level indicates a fault had occurred, external pull-up to MCU power supply is needed (1kΩ to 10kΩ).
MODE	3	I	—	—
ISET	4	I	Driver current set	Gate driver output current setting, set by an external resistor.
DRVHA	5	O	Gate driver	Gate driver output for bridge A high-side.
SRCHA	6	I	Source connection	Source connection for bridge A high-side.
COM	7	I/O	Common for 3-driver	Common source connection for 3 lower side drivers, suggested to connect to power ground.
DRVLA	8	O	Gate driver	Gate driver output for bridge A low-side.
DRVLB	9	O	Gate driver	Gate driver output for bridge B low-side.
SRCHB	10	I	Source connection	Source connection for bridge B high-side.
DRVHB	11	O	Gate driver	Gate driver output for bridge B high-side.
DRVHC	12	O	Gate driver	Gate driver output for bridge C high-side.
SRCHC	13	I	Source connection	Source connection for bridge C high-side.
DRVLC	14	O	Gate driver	Gate driver output for bridge C low-side.
VGLS	15	P	Low-side gate driver power supply	Internal voltage regulator for low-side gate driver, connecting 1μF and 10nF capacitor to GND.
VHP	16	P	High-side gate driver power supply	Internal charge pump for high-side gate driver, connecting 1μF capacitor to VP.
HCP	17	P	Charge pump flying capacitor	Flying capacitor for charge pump, connecting 47nF capacitor between HCP and LCP.
LCP	18			
VP	19	P	Power supply voltage	High-side MOSFET drain connection; common for all three half bridges, connecting

Pin Name	Pins	Pin Type	Functions Description	
				4.7uF capacitor to GND.
BST	20	P	Input for bootstrap capacitor	An external capacitor is required between the BST and the SW pins to provide bias to the MOSFET gate driver.
BDRV	21	O	Gate drive	Buck circuit, connecting to the gate terminal of the external MOSFET switch.
SW	22	P	Switching node	Buck circuit, connecting to the source terminal of the external MOSFET switch.
CS	23	I	Current sense	Buck circuit, current sense voltage input.
FB	24	I	Regulated output	Buck circuit, connecting directly to the regulated output voltage.
VDD	25	P	Voltage Regulator	5V internal supply regulator, connecting 6.3V, 1μF ceramic capacitor to GND.
nSD	26	I	Buck controller enable	Internal pull-down, pull above 2.2V to enable.
PWMHA	27	I	PWM input	Logic input signal for bridge A high-side.
PWMLA	28	I	PWM input	Logic input signal for bridge A low-side.
PWMHB	29	I	PWM input	Logic input signal for bridge B high-side.
PWMLB	30	I	PWM input	Logic input signal for bridge B low-side.
PWMHC	31	I	PWM input	Logic input signal for bridge C high-side.
PWMLC	32	I	PWM input	Logic input signal for low-side bridge C.
GND	Thermal	P	Device ground	Must be connected to ground.

Notes:

Type: I = input, O = output, P = power, OD = open drain.

The table below shows the pin definition of GD30DR8304x.

Table 4-3. GD30DR8304x pin configuration

Pin Name	Pins	Pin Type	Functions Description	
PWMLC	1	I	PWM input	Logic input signal for low-side bridge C.
ENGATE	2	I	Enable gate driver	Enables the gate driver, internal pull-down.
nFAULT	3	OD	Fault indicator	The low level indicates a fault had occurred, external pull-up to MCU power supply is needed (1kΩ to 10kΩ).
DRVHA	4	O	Gate driver	Gate driver output for bridge A high-side.
SRCHA	5	I	Source connection	Source connection for bridge A high-side.
DRVLA	6	O	Gate driver	Gate driver output for bridge A low-side.
DRVLB	7	O	Gate driver	Gate driver output for bridge B low-side.
SRCHB	8	I	Source connection	Source connection for bridge B high-side.
DRVHB	9	O	Gate driver	Gate driver output for bridge B high-side.
DRVHC	10	O	Gate driver	Gate driver output for bridge C high-side.
SRCHC	11	I	Source connection	Source connection for bridge C high-side.
DRVLC	12	O	Gate driver	Gate driver output for bridge C low-side.
VGLS	13	P	Low-side gate driver power supply	Internal voltage regulator for low-side gate driver, connecting 1μF and 10nF capacitor to GND.
VHP	14	P	High-side gate driver power supply	Internal charge pump for high-side gate driver, connecting 1μF capacitor to VP.
HCP	15	P	Charge pump flying capacitor	Flying capacitor for charge pump, connecting 47nF capacitor between HCP and LCP.
LCP	16			
VP	17	P	Power supply voltage	High-side MOSFET drain connection; common for all three half bridges, connecting 4.7uF capacitor to GND.
VDD	18	P	Voltage Regulator	5V internal supply regulator, connecting 6.3V, 1μF ceramic capacitor to GND.
NC	19	—	—	This pin is not connected to silicon.
PWMHA	20	I	PWM input	Logic input signal for bridge A high-side.
PWMLA	21	I	PWM input	Logic input signal for bridge A low-side.

Pin Name	Pins	Pin Type	Functions Description	
PWMHB	22	I	PWM input	Logic input signal for bridge B high-side.
PWMLB	23	I	PWM input	Logic input signal for bridge B low-side.
PWMHC	24	I	PWM input	Logic input signal for bridge C high-side.
GND	Thermal	P	Device ground	Must be connected to ground.

Notes:

Type: I = input, O = output, P = power, OD = open drain.

5. Functional description

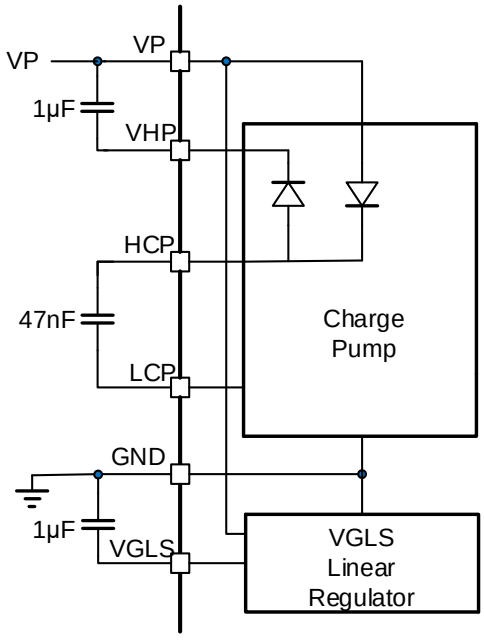
5.1. Power module

5.1.1. Charge pump and VGLS_LDO

A charge pump supplying voltage for the high-side gate driver is integrated to generate the appropriate gate to source bias voltage for the external high-side NMOSFET across a wide input supply voltage range. The charge pump generates $V_{VHP} = 2 \times V_{VP} - 1.5V$ in doubled mode when V_{VP} is less than 11.5V and regulates the V_{VHP} supply to $V_{VP}+10V$ when V_{VP} is larger than 11.5V, respectively. The charge pump requires a 1μF capacitor between the VP and VHP pins and a 47nF capacitor between the HCP and LCP pins to act as the storage capacitor and flying capacitor, respectively. An undervoltage monitor for charge pump is integrated to detect the undervoltage condition.

A 11V linear regulator, which operates from the VP voltage supply input, supplying voltage for the low-side gate driver is integrated to generate the correct gate to source voltage for the external low-side NMOSFET. The linear regulator supporting an output current of 40 mA requires a 1μF capacitor between the VGLS and GND pins to act as the regulated capacitor.

Figure 5-1. Charge pump and VGLS_LDO



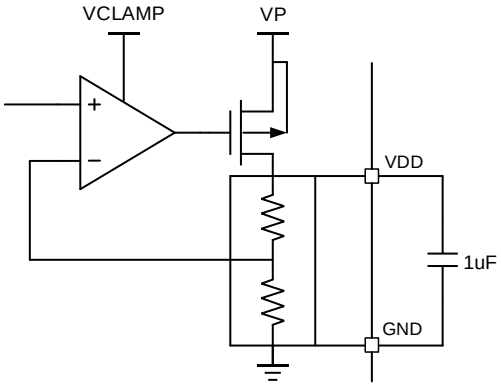
5.1.2. VDD_LDO

A linear regulator outputting 5V, is integrated to supply part of the chip and external circuits or MCU.

The output driving current is 40mA, when output current exceeds 40mA, the output value will drop significantly.

When the ENGATE pin is driven to low, the chip works in sleep mode to save power, which supplies 10mA current.

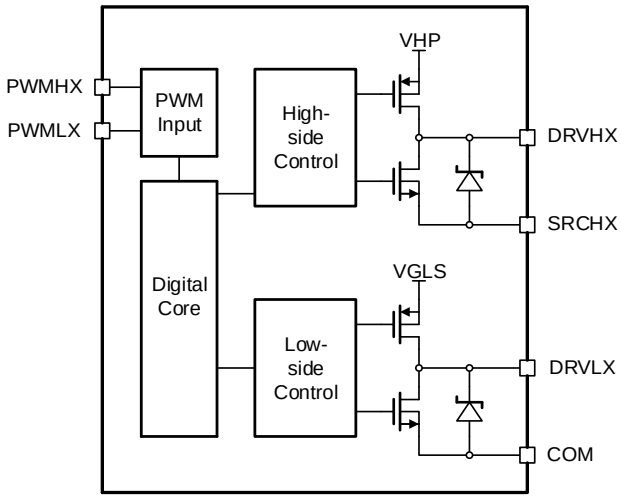
Figure 5-2. VDD_LDO



5.2. Gate driver architecture

The gate driver uses a push-pull topology in both the high-side and low-side providing a strong pull up or down to the external NMOSFET gates. And it uses a programmable current control scheme through 4 level input pin to adjust the peak gate drive current, so the VDS slew rate of the external power MOSFETs can be smart-adaptable. Both sides of the gate driver incorporate Zener clamp diodes to protect the external NMOSFETs gates from overvoltage scenarios.

Figure 5-3. Gate driver architecture



5.3. Gate driver control mode

The GD30DR830x is a gate driver IC designed for three-phase motor driver applications, operating in a wide range of 4.5V to 30V. This device integrates three half-bridge drivers, which can operate in only one methods: 6xPWM mode.

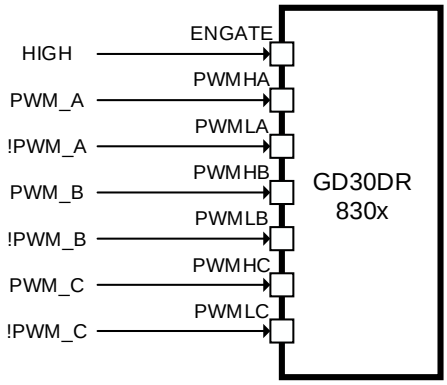
5.3.1. 6xPWM Mode

The 6xPWM mode relates 6 inputs (PWMHx and PWMLx) to the 6 gate drives (DRVHx and DRVLx), and each half-bridge supports three output states: low, high, or high-impedance (Hi-Z). The corresponding PWMHx and PWMLx signals control the output state as listed in ***Table 5-1. 6xPWM mode truth table***.

Table 5-1. 6xPWM mode truth table

PWMLx	PWMHx	DRVLx	DRVHx	SRCHx
0	0	L	L	Hi-Z
0	1	L	H	H
1	0	H	L	L
1	1	L	L	Hi-Z

Figure 5-4. 6xPWM mode



5.4. Gate driver slew rate control

The high-side and low-side peak gate drive currents are programmable through the external resistors connected to the level pin (ISET), so the VDS slew rate can be smart-adaptable to different external power MOSFETs. A proprietary slew rate is implemented to the MOSFETs to improve the system EMI.

5.5. Dead time

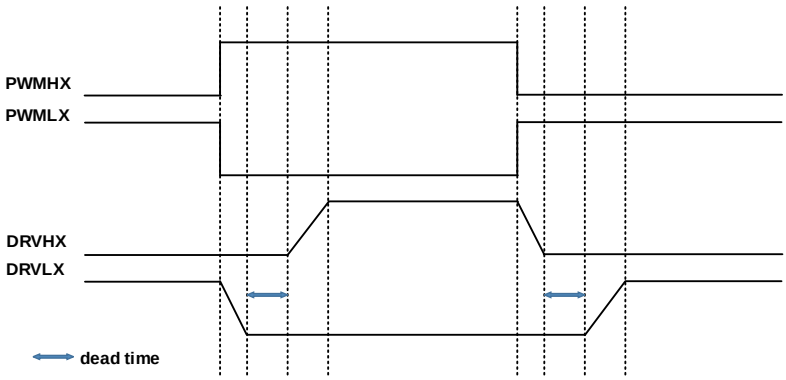
An internal handshaking scheme is used to prevent shoot-through and minimize the dead time when MOSFETs state in each half-bridge varies.

The dead time insertion is available in 6xPWM mode.

The applying dead time can be expressed as below:

$$\text{dead time} = 200\text{ns}$$

Figure 5-5. Dead time insertion



5.6. Device configuration

The GD30DR8306x device can use external resistor connected to configuring pins to set the device configuration.

5.6.1. Hardware interface

The Hardware interface is available in GD30DR8306x device. That uses external resistor connected to designated pins to set the device configuration, such as PWM MODE and the gate driver current.

The MODE pin configures the PWM control mode.

Table 5-2. PWM mode configuration table

External interface	Mode selection
Hi-Z	6xPWM mode

The ISET pin configures the gate driver source/sink current.

Table 5-3. Gate drive current configuration table

External interface	Sink	Source
Tied to GND	75mA	50mA
47KΩ±5% to GND	300mA	250mA
Hi-Z	600mA	500mA
Tied to VDD	1.2A	1A

5.7. Over temperature protection

If the die temperature exceeds the trip point of the thermal limit (T_{OTSD}), the nFAULT pin is driven to low, which indicates a thermal event occurred until a clear fault command is issued through an effective falling edge on ENGATE pin (t_{RST}).

5.8. Buck Controller

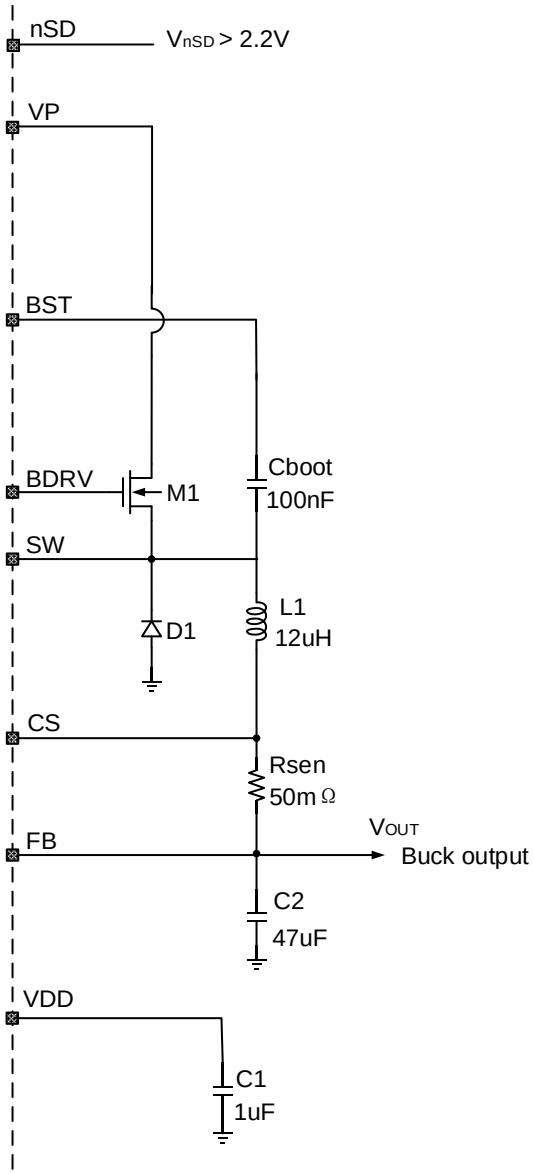
A DC/DC buck controller is integrated in GD30DR8306x, the controller drives an external high side N-channel MOSFET for 2A output current, the output is regulated to 5V. The controller requires an external schottky diode to conduct current when the high side MOSFET is off.

The controller method is based upon peak current mode control and the switching frequency is 500kHz. A small ceramic capacitor Cboot is required between BST and SW pin to provide the gate drive voltage for the high side MOSFET. The Cboot capacitor is refreshed when the high side MOSFET is off and the low side diode conducts and the BST to SW voltage is charged to approximately 4.5V. When the voltage from BST to SW drops below 2.2V, the high side MOSFET is turned off using an UVLO circuit which allows the low side diode to conduct and refresh the charge on the Cboot capacitor. An internal circuit will also turn off the high side MOSFET and pull SW voltage to ground every four switching cycles for approximately 180ns to recharge the Cboot capacitor in maximum duty cycle applications or when the load is light.

The controller requires an external 50mΩ resistor between CS and FB pin for current sensing. To ensure the control loop stability, an output capacitor in the range of 20uF-100uF is recommended and the ESR should be less than 150 mΩ. ***Figure 5-6. Buck controller application circuit*** shows a typical application circuit.

Note: Only GD30DR8306x with buck controller.

Figure 5-6. Buck controller application circuit



6. Electrical characteristics

6.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 6-1. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
Gate driver				
V_{VP}	Power supply pin voltage (VP)	-0.3	30	V
V_{VHP}	Charge pump pin voltage (HCP, VHP)	-0.3	V_{VP} + 12	V
V_{LCP}	Charge pump negative-switching pin voltage (LCP)	-0.3	V_{VP}	V
V_{VDD}	Internal logic regulator pin voltage (VDD)	-0.3	5.5	V
V_I	Digital pin voltage (ENGATE, PWMHx, PWMLx, nFAULT, MODE, ISET)	-0.3	5.5	V
V_{DRVH}	Continuous high-side gate drive pin voltage (DRVHx)	-2	V_{VHP} + 0.5	V
V_{DRVH}	Transient 200-ns high-side gate drive pin voltage (DRVHx)	-3	V_{VHP} + 0.5	V
V_{DRVH}	High-side gate drive pin voltage with respect to SRCHx (DRVHx)	-0.3	13.5	V
V_{SRCH}	Continuous high-side source sense pin voltage (SRCHx)	-1	V_{VP} + 5	V
V_{DRVL}	Continuous low-side gate drive pin voltage (DRVLx)	0.5	13.5	V
I_{SRC}	Gate drive pin source current (DRVHx, DRVLx)	Internally limited		A
I_{SNK}	Gate drive pin sink current (DRVHx, DRVLx)	Internally limited		A
V_{COM}	Continuous low-side source sense pin voltage (COM)	-0.6	1	V
Buck controller(GD30DR8306x only)				
V_{BDRV}	Power supply pin voltage (BDRV)	-0.3	30	V
V_{nSD}	Shutdown control pin voltage (nSD)	-0.3	V_{VP}	V
V_{FB}	Voltage feedback pin voltage (FB)	-0.3	7	V
V_{BST}	Bootstrap pin voltage with respect to SW (BST)	-0.3	7	V
V_{SW}	Switching node pin voltage (SW)	-0.3	V_{VP}	V
V_{CS}	Current Sense (CS)	-0.3	7	V
Thermal characteristics				
T_J	Operating junction temperature	-40	125	°C
T_{stg}	Storage temperature	-65	150	°C

6.2. Recommended operation conditions

Table 6-2. Recommended operation conditions

Symbol	Parameter	Min	Max	Unit
Gate driver and current sense amplifier				
V_{VP}	Power supply voltage (VP)	4.5	30	V
V_I	Input voltage (ENGATE, PWMHx, PWMLx, nFAULT, MODE, ISET)	0	5.5	V
f_{PWM}	Applied PWM signal (PWMHx, PWMLx)	0	200	kHz
I_{GATE_HS}	High-side average gate drive current (DRVHx)	0	25	mA
I_{GATE_LS}	Low-side average gate drive current (DRVLx)	0	25	mA
I_{DVDD}	External load current (VDD)	0	40	mA
V_{VDD}	Reference voltage input (VDD)	3	5.5	V
V_{OD}	Open drain pull-up voltage (nFAULT)	0	5.5	V
I_{OD}	Open drain output current (nFAULT)	0	5	mA
Buck controller(GD30DR8306x only)				
V_{BDRV}	Drive voltage (BDRV)	4.5	30	V
V_{nSD}	Shutdown control input voltage (nSD)	0	30	V
Thermal characteristics				
T_A	Operating ambient temperature	-40	105	°C

6.3. Power supplies and current consumption

Table 6-3. Power supplies and currents

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VP}	VP operating supply current	V_{VP} = 24 V, EN = 3.3 V, PWMHx/PWMLx = 0 V	10.5	—	14	mA
I_{VPQ}	VP sleep mode supply current	ENGATE = nSD = 0 V, V_{VP} = 30 V	108	144	200	μA
t_{RST}	Reset pulse time	ENGATE = 0 V period to reset faults	8	—	40	μs
t_{WAKE}	Turn on time	V_{VP} > V_{UVLO}, ENGATE = 3.3 V to outputs ready	1	—	—	ms
t_{SLEEP}	Turn off time	ENGATE = 0 V to device sleep mode	1	—	—	ms
V_{VDD}	VDD regulator voltage	I_{VDD} = 0 to 40 mA	—	5	—	V
V_{VHP}	VHP operating voltage with respect to VP	V_{VP} = 12 V, I_{VHP} = 0 to 25 mA	8.4	11	12.5	V
		V_{VP} = 8 V, I_{VHP} = 0 to 20 mA	6.3	9	10	
		V_{VP} = 6 V, I_{VHP} = 0 to 15 mA	4	5	6	
		V_{VP} = 4.5 V, I_{VHP} = 0 to 10 mA	4	5	6	
V_{VGLS}	Low-side gate drive voltage with respect to GND	V_P = 16 V	10.5	11.2	11.5	V

6.4. Logic inputs characteristics

Logic input pins include ENGATE, PWMHx, PWMLx.

Table 6-4. Logic input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input logic low voltage	—	0	—	0.8	V
V_{IH}	Input logic high voltage	—	1.5	—	5.5	V
V_{HYS}	Input logic hysteresis	—	100	—	—	mV
I_{IL}	Input logic low current	V_{VIN} = 0 V	-5.5	—	5.5	μA
I_{IH}	Input logic high current	V_{VIN} = 5 V	—	50	100	μA
R_{PD}	Pull-down resistance	To GND	100	—	—	kΩ

6.5. Open drain outputs characteristics

Open drain output pins include nFAULT.

Table 6-5. Open drain output characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output logic low voltage	I_O = 5 mA	—	—	0.1	V
I_{OZ}	Output high impedance leakage	V_O = 5 V	-5.5	0.01	5.5	μA

6.6. Gate driver characteristics

Gate driver pins include DRVHx, DRVLx.

Table 6-6. Gate driver characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{DTF}	Gate drive dead time (Fixed)	—	—	200	—	ns
I_{SRC}	Peak source gate current	Tied to GND	—	50	—	mA
		47KΩ±5% to GND	—	250	—	
		Hi-Z	—	500	—	
		Tied to VDD	—	1000	—	
I_{SNK}	Peak sink gate current	Tied to GND	—	75	—	mA
		47KΩ±5% to GND	—	300	—	
		Hi-Z	—	600	—	
		Tied to VDD	—	1200	—	
R_{OFF}	Gate hold off resistor	DRVHx to SHx and DRVLx to GND	—	150	—	kΩ

6.7. VDD LDO characteristics

Table 6-7. VDD LDO characteristics

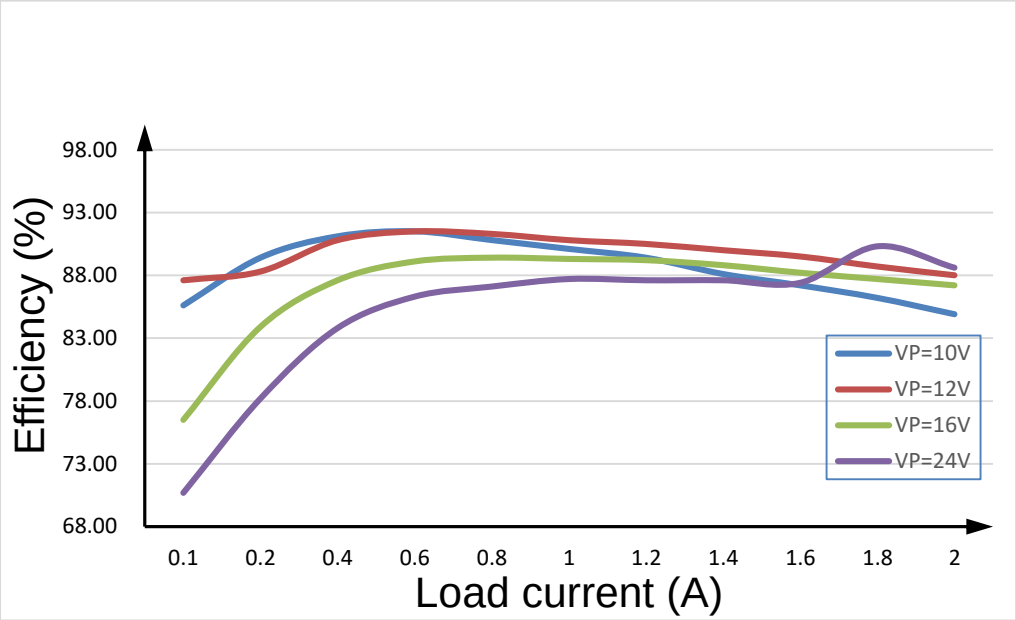
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDD}	LDO output voltage and Internal logic voltage	—	4.8	5.1	5.2	V
V_{UVLO}	VP undervoltage lockout	VP falling, UVLO	4.2	4.3	4.5	V
V_{UVLO_HYS}	VP undervoltage hysteresis	Rising to falling threshold	—	200	—	mV
t_{UVLO_DEG}	VP undervoltage deglitch time	VP falling, UVLO	—	10	—	μs

6.8. Buck controller characteristics

Table 6-8. Buck controller characteristics(GD30DR8306x only)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OUT}	Buck Controller output voltage	—	—	5.0	—	V
I_Q	Shutdown supply current	V_{nSD} = 0 V	—	6	10	μA
V_{nSD_H}	Rising nSD threshold	—	—	2.2	—	V
V_{nSD_L}	Falling nSD threshold	—	—	0.8	—	V
R_{PD}	nSD pull-down resistor	—	—	9	—	MΩ
T_{SS}	Soft start time	—	—	1	—	ms
T_{on_min}	Minimum on time	—	—	35	—	ns
T_{OFF}	Forced off time	—	—	180	—	ns
T_R	BDRV rise time(10%~90%)	C_L = 1000pF	—	25	—	ns
T_F	BDRV fall time(90%~10%)	C_L = 1000pF	—	20	—	ns
I_{OH}	Peak BDRV source current	—	—	300	—	mA
I_{ol}	Peak BDRV sink current	—	—	450	—	mA
F_{SW}	Switching frequency	—	450	500	550	kHz
I_{LIMIT}	Peak current limit	V_{VP} = 24 V	—	4.2	—	A
V_{UVP}	V_{OUT} UVP threshold rise edge	—	—	3.24	—	V
	V_{OUT} UVP threshold fall edge		—	3.0	—	V
V_{OVP}	V_{OUT} OVP threshold	—	—	5.5	—	V
V_{UVLO}	BST UVLO voltage	BST to SW	—	2.2	—	V
D_{MAX}	Maximum duty cycle	—	—	97%	—	—

Figure 6-1. Buck controller efficiency diagram



6.9. Protection features

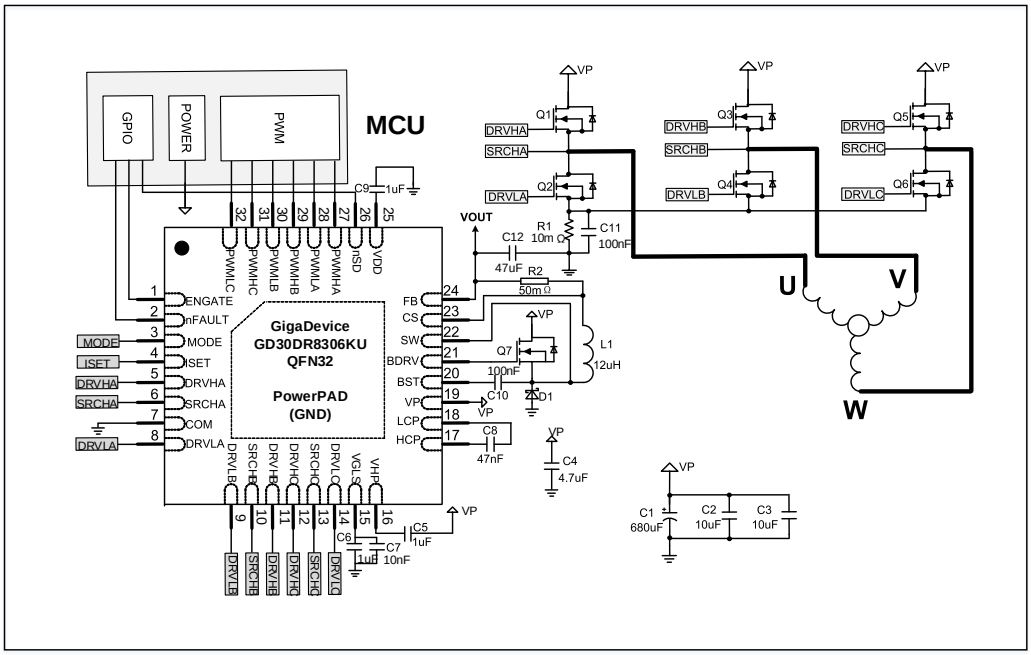
Protection features include over current protection, under voltage lockout and thermal shutdown.

Table 6-9. Protection features characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{UVLO}	VP undervoltage lockout	VP rising, UVLO	4.2	4.3	4.4	V
		VP falling, UVLO	4.0	4.1	4.2	
V_{UVLO_HYS}	VP undervoltage hysteresis	Rising to falling threshold	—	200	—	mV
t_{UVLO_DEG}	VP undervoltage deglitch time	VP falling, UVLO	—	100	—	μs
VHP_{UV}	Charge pump undervoltage lockout	VHP falling, relative to VP	—	2.8	—	V
VLP_{UV}	Charge pump undervoltage lockout	VLP falling, relative to GND	—	2.8	—	V
T_{OTSD}	Thermal shutdown temperature	Die temperature, T_J	150	170	185	°C
T_{HYS}	Thermal hysteresis	Die temperature, T_J	—	20	—	°C

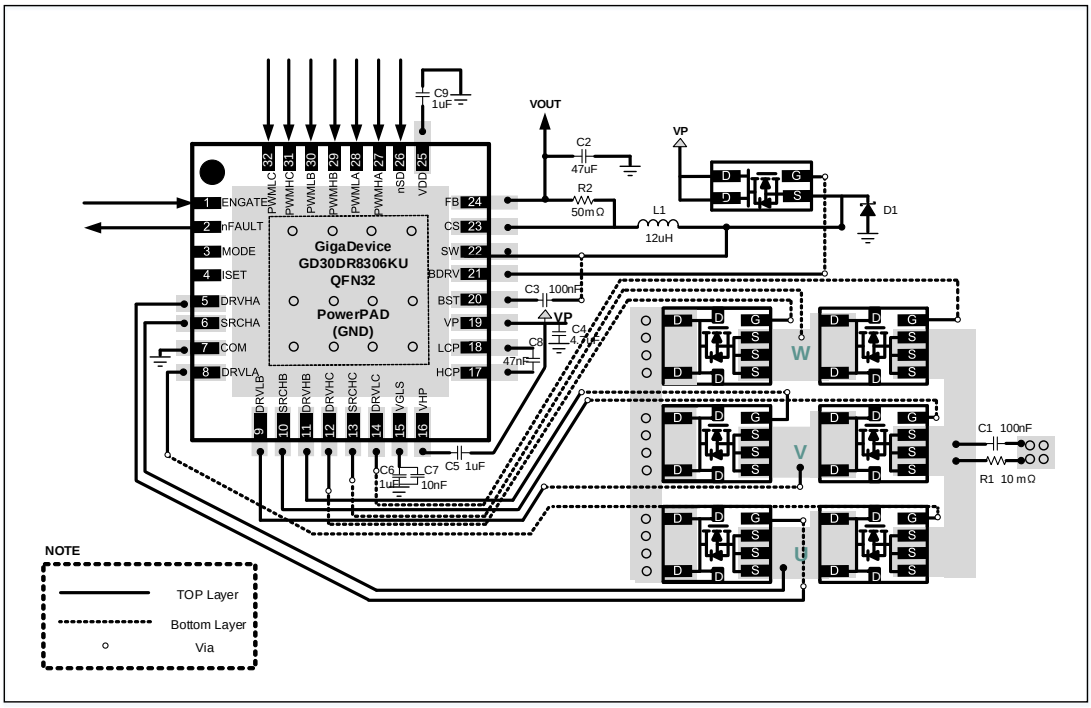
7. Typical application circuit

Figure 7-1. Typical application circuit for GD30DR8306x



8. Layout guideline

Figure 8-1. Typical layout guideline



Notes:

1) The VDD 1uF bypass capacitors should connect directly the VSS to ensure loop stability.
2) The VP 4.7uF bypass capacitor should be placed close to the supply pin with a direct path back to the GND pad.
3) The VP and VHP 1uF bypass capacitors should connect to the charge pump pins.
4) The VGLS 1uF and 10nF capacitor should connect directly the GND net to ensure loop stability.
5) The HCP and LCP 47nF flying capacitor should be placed directly next to the charge pump pins.
6) All capacitors should be as close to the chip pin as possible.

9. Package information

9.1. QFN32 package outline dimensions

Figure 9-1. QFN32 package outline

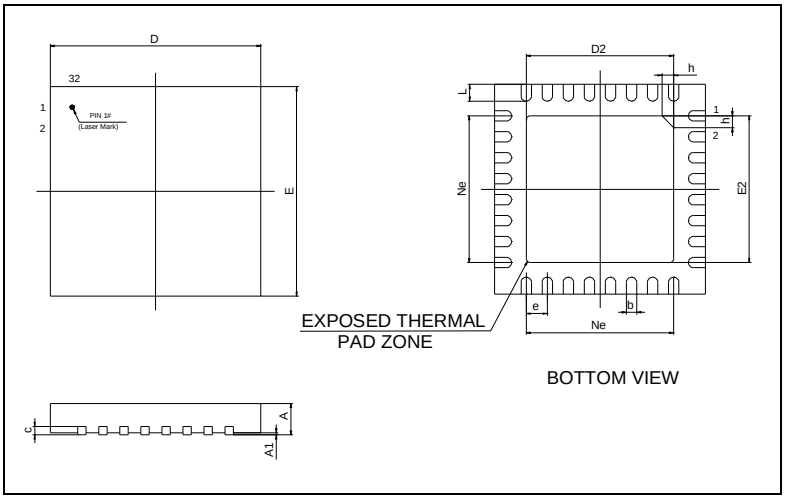
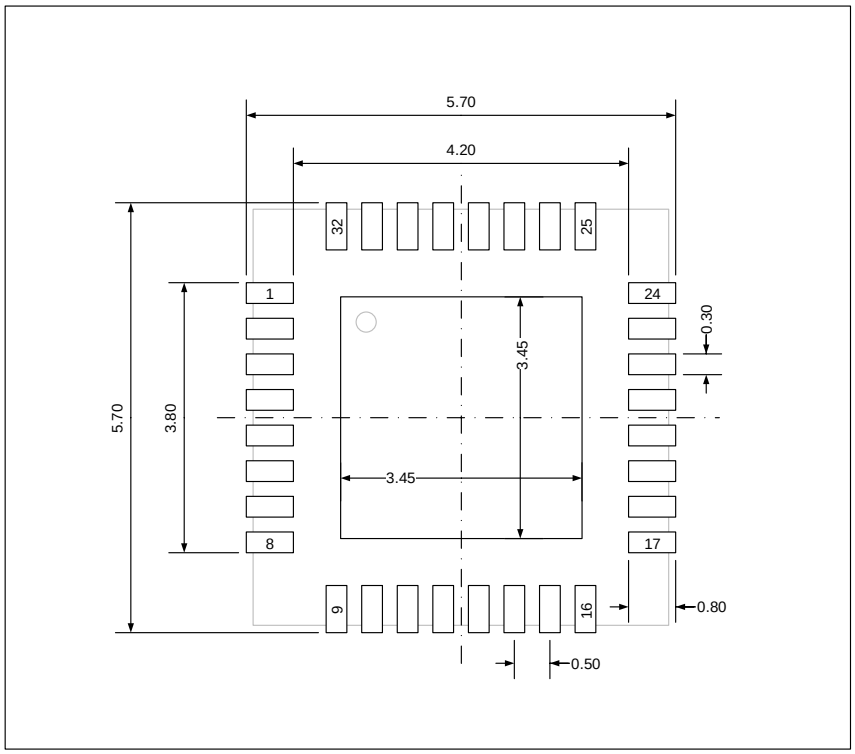


Table 9-1. QFN32 dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
e	—	0.50	—
h	0.30	0.35	0.40
L	0.35	0.40	0.45
Ne	—	3.50	—

(original dimensions are in millimeters)

Figure 9-2. QFN32 recommended footprint



(All dimensions are in millimeters)

9.2. QFN24 package outline dimensions

Figure 9-3. QFN24 package outline

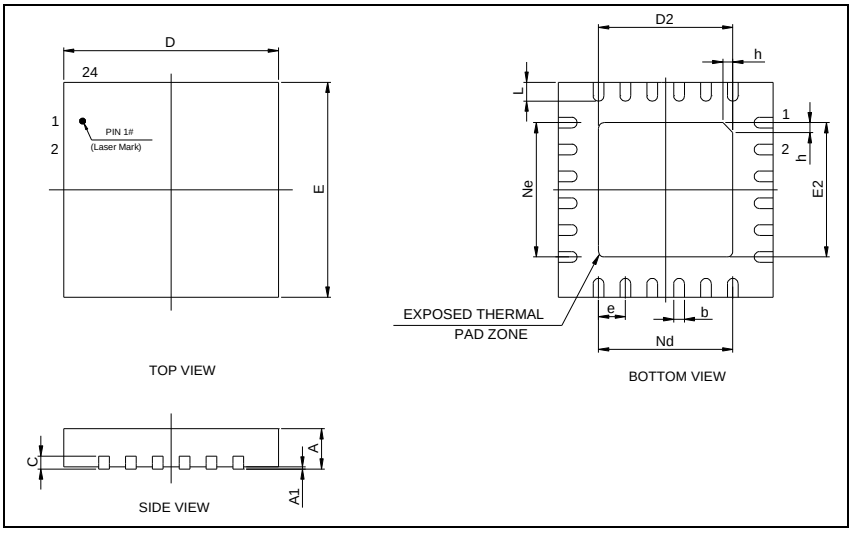
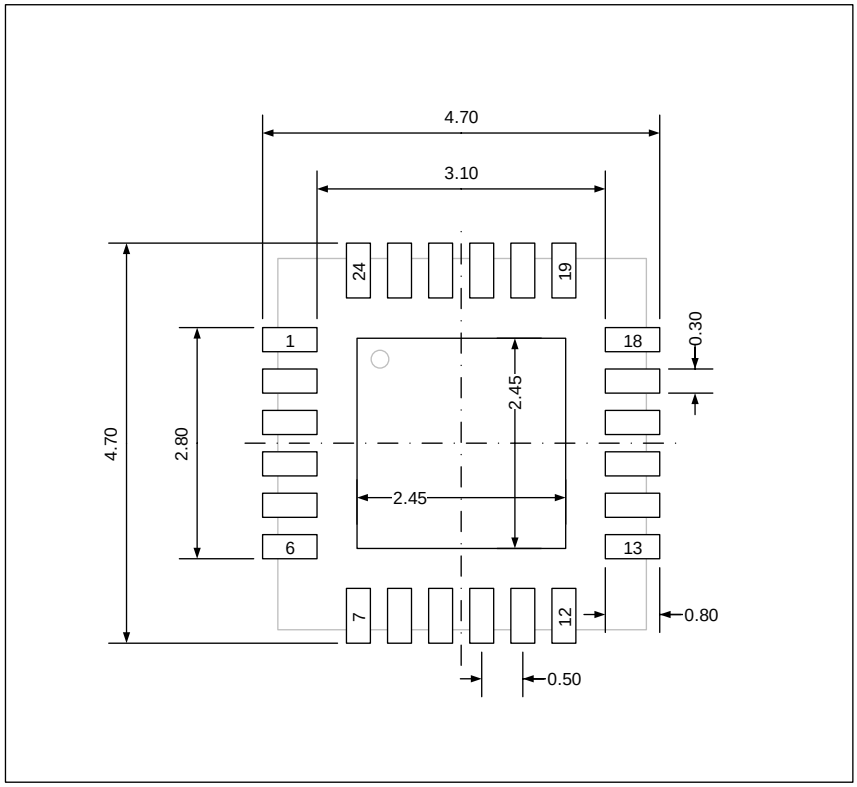


Table 9-2. QFN24 dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
e	—	0.50	—
h	0.30	0.35	0.40
L	0.35	0.40	0.45
Nd	—	2.50	—
Ne	—	2.50	—

(Original dimensions are in millimeters)

Figure 9-4. QFN24 recommended footprint



(All dimensions are in millimeters)

9.3. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "Θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

Θ_{JA}: Thermal resistance, junction-to-ambient.

Θ_{JB}: Thermal resistance, junction-to-board.

Θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$\Theta_{JA} = (T_J - T_A)/P_D$

$\Theta_{JB} = (T_J - T_B)/P_D$

$\Theta_{JC} = (T_J - T_C)/P_D$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

Θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower Θ_{JA} can be considerate as better overall thermal performance. Θ_{JA} is generally used to estimate junction temperature.

Θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

Θ_{JC} represents the thermal resistance between the chip surface and the package top case. Θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 9-3. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
Θ_{JA}	Natural convection, 2S2P PCB	QFN32	38.5	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	QFN32	10.04	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	QFN32	14.67	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	QFN32	10.78	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	QFN32	0.46	°C/W
Symbol	**Condition**	**Package**	**Value**	**Unit**
Θ_{JA}	Natural convection, 2S2P PCB	QFN24	47.51	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	QFN24	14.9	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	QFN24	20.99	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	QFN24	15.05	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	QFN24	0.86	°C/W

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

10. Ordering information

Table 10-1. Part ordering code for GD30DR8306x device

Ordering Code	Package	Package Type	Packing Type	MOQ	Temperature Operating Range
GD30DR8306KU	QFN32(5X5)	Green	Tray	2940	Industrial -40°C to +105°C
GD30DR8304EUTR	QFN24(4X4)	Green	Tape&Reel	3000	Industrial -40°C to +105°C

Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the “Product”), is owned by the Company according to the laws of the People’s Republic of China and other applicable laws. The Company reserves all rights under such laws and no Intellectual Property Rights are transferred (either wholly or partially) or licensed by the Company (either expressly or impliedly) herein. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

The Company makes no representations or warranties of any kind, express or implied, with regard to the merchantability and the fitness for a particular purpose of the Product, nor does the Company assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the sole responsibility of the user of this document to determine whether the Product is suitable and fit for its applications and products planned, and properly design, program, and test the functionality and safety of its applications and products planned using the Product. Unless otherwise expressly specified in the datasheet of the Product , the Product is designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and the Product is not designed or intended for use in (i) safety critical applications such as weapons systems, nuclear facilities, atomic energy controller, combustion controller, aeronautic or aerospace applications, traffic signal instruments, pollution control or hazardous substance management; (ii) life-support systems, other medical equipment or systems (including life support equipment and surgical implants); (iii) automotive applications or environments, including but not limited to applications for active and passive safety of automobiles (regardless of front market or aftermarket), for example, EPS, braking, ADAS (camera/fusion), EMS, TCU, BMS, BSG, TPMS, Airbag, Suspension, DMS, ICMS, Domain, ESC, DCDC, e-clutch, advanced-lighting, etc.. Automobile herein means a vehicle propelled by a self-contained motor, engine or the like, such as, without limitation, cars, trucks, motorcycles, electric cars, and other transportation devices; and/or (iv) other uses where the failure of the device or the Product can reasonably be expected to result in personal injury, death, or severe property or environmental damage (collectively "Unintended Uses"). Customers shall take any and all actions to ensure the Product meets the applicable laws and regulations. The Company is not liable for, in whole or in part, and customers shall hereby release the Company as well as its suppliers and/or distributors from, any claim, damage, or other liability arising from or related to all Unintended Uses of the Product. Customers shall indemnify and hold the Company, and its officers, employees, subsidiaries, affiliates as well as its suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Product.

Information in this document is provided solely in connection with the Product. The Company reserves the right to make changes, corrections, modifications or improvements to this document and the Product described herein at any time without notice. The Company shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. Information in this document supersedes and replaces information previously supplied in any prior versions of this document.